A Trapezoidal Cross-Section Stacked Gate FinFET with Gate Extension for Improved Gate Control

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***Abstract*—An improved trapezoidal pile gate bulk FinFET device is implemented with an extension in the gate for enhancing the performance. The novelty in the design is trapezoidal cross-section FinFET with stacked metal gate along with extension on both sides. Such improved device structure with additional process cost exhibits significant enhancement in the performance metrics specially in terms of leakage current behavior. The simulation study proves the suitability of the device for low power applications with improved on/off current ratio, subthreshold swing (SS), drain induced barrier lowering (DIBL), Gate Induced Drain Leakage (GIDL) uniform distribution of electron charge density along the channel and effects of Augur recombination within the channel.**

***Keywords*—Drain Induced Barrier Lowering (DIBL); Gate Induced Drain Leakage (GIDL); Subthreshold Swing (SS); Silicon On-Insulator (SOI)**

I. Introduction

Introduction of FinFET in 2011 revolutionized the way in which transistors were built [1]. It is the most promising device structure to meet the challenges of low power, high density, high speed and multi-operational capability applications [2]. With transformations in the fabrication technology and increased focus on improving electrical properties, different variants of FinFETs have been suggested by the Integrated Circuit (IC) designers around the world. These include GAA-Gate All Around, MuG- Multi-Gate, Tri-Gate, Pi/Omega Gate FinFET, and SOI-Silicon-on-Insulator [2][3]–[8][9][10].

Beyond 22nm, short channel effects predominantly hamper device performance due to fringing electric field within the channel resulting from loss of gate control. Approaches to address this issue have included use of high K dielectric maintaining effective oxide thickness, controlling charge transport through the channel by using strained gate or by the addition of spacers to form shallow, intermediate and deep junction areas, and metal gate work function engineering by using gate stack technique [11][12]. Introduction of a gate stringer along the source-drain extension acts as a subthreshold leakage suppressor in bulk FinFET [13].

In this paper we have implemented a new FinFET design utilizing the advantages of both gate stack engineering and a gate stringer. With Intel's revelation [14] of non-vertical sidewalls of the fins, we have chosen a trapezoidal cross-section for this new design as opposed to existing attempts which have solely focused on rectangular cross-section FinFETs. Adhering to the standard device design guidelines, a mask layout has been designed using K-layout open source layout editor tool for the new FinFET (as shown in Fig. 1(a). The implemented 3-D FinFET structure is indicated in Fig. 1(b).

II. Device Description and Simulation Details

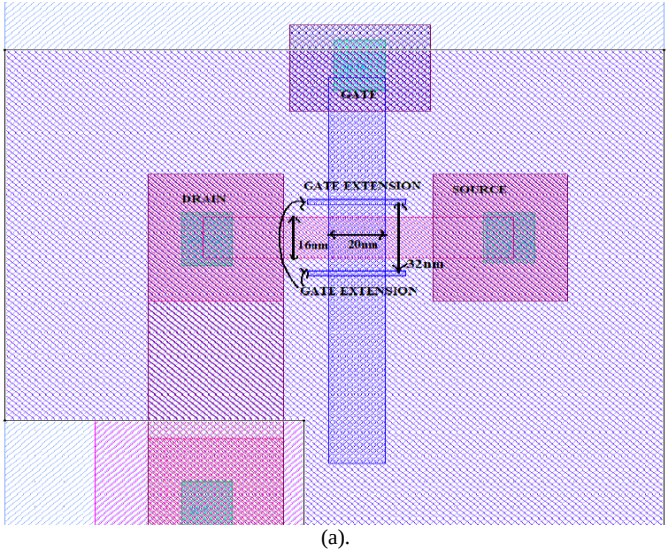
A. Device Design Specifications

This new design has been implemented using cost and thermal stability advantage of Si Bulk technology.

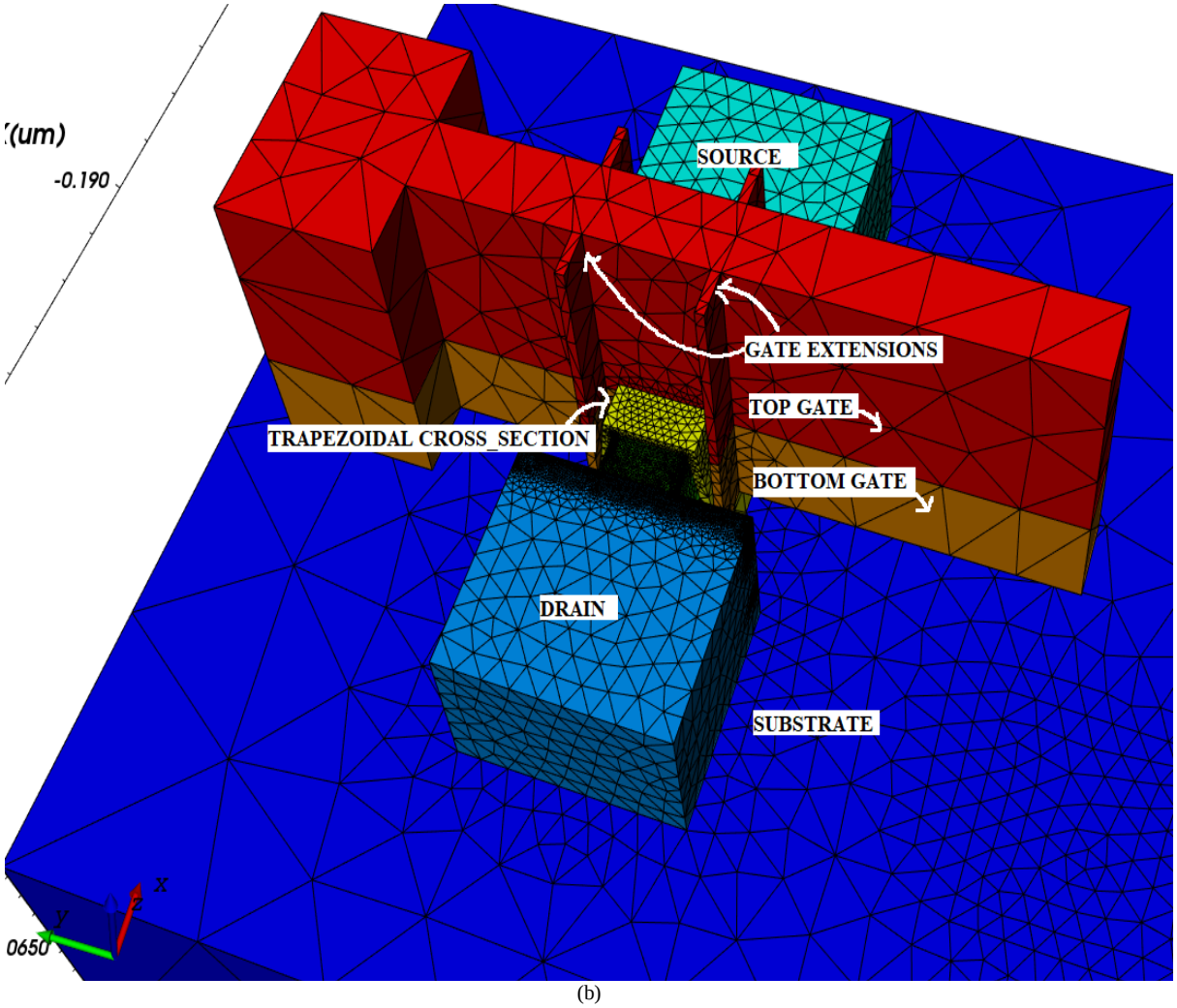
The well doping concentration is 10^{18}cm^{-3} and source/drain doping concentration is 10^{20}cm^{-3}. Device specifications have been selected referring to the practical implementation literature available [15]–[18]. Considering the doping profile, width of the fin is 20 nm and height of the fin is 30nm.The effective width of the fin is $W_{eff} = 2H_{fin} + W_{fin} = 2(30nm) + 20 = 80nm$[6]. The separation between the two gate extensions is 32 nm. Metal gate work functions for bottom and top gates are 4.5eV and 5.1 eV, respectively. The permittivity of the high K-dielectric is 21.

B. Drain Current Modelling

The current density equations and Poisson equations used to derive drain current through energy balanced in drift and diffusion modelling in the 3-D device simulation tool is given by:



(a).



(b)

Fig. 1. (a) Mask Layout for the Stacked Gate FinFET with Gate Extension, (b) 3D Structure of the New FinFET with Stacked Gate Stringer (Gate Extension)..

$$\overrightarrow{J_n} = q\mu_n n\overrightarrow{E_n} + \mu_n k_b\,(n \cdot \nabla T_n + \nabla n \cdot T_n) \quad (1)$$

$$\overrightarrow{J_p} = q\mu_p p\overrightarrow{E_p} - \mu_p k_b\,(p \cdot \nabla T_p + \nabla p \cdot T_p) \quad (2)$$

where ∇T_n *and* ∇T_p are electron and hole temperature. The Drain current model considers thermal as well as kinetic energy for total energy computation.

To investigate the electrostatic characteristics, the ambient temperature has been assumed to be 300K. The Lucent mobility model has been used to model the mobility of charge carriers. The Lucent model considers bulk mobility, surface mobility as well as mobility due to applied electrical field in both perpendicular and lateral directions as given by equation [19].

$$\mu_0 = \left[\frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}}\right]^{-1} \quad (3)$$

where μ_b is bulk mobility and μ_{ac} and μ_{sr} denote electric field and surface mobility components, respectively.

To validate the performance of the new FinFET (Device A), its comparative analysis has been carried out with respect to a similar FinFET without gate stringer (Device B).

Drain current values have been varied from 0 to 1V for keeping drain to source voltage constant at 0.05V for linear region of operation and 0.5V for saturation region of operation. A plot of drain current variation on logscale with respect to gate voltage is indicated in Fig. 2. Significant improvement in on/off current ratio is observed in device A.

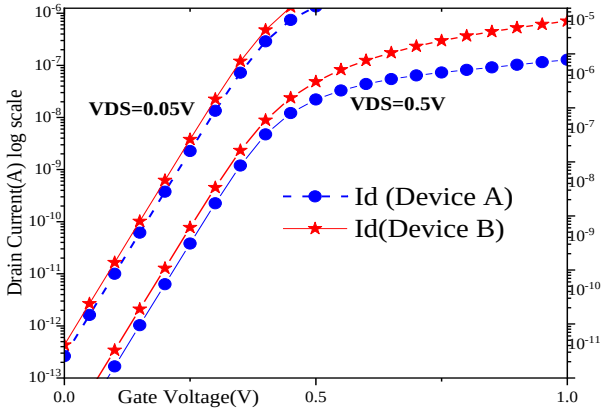


Fig. 2. Gate Voltage Vs Drain Current Characteristics for Stacked and Extended Gate Stacked FinFET.

C. Perfromance Metrics

For low power applications, Subthreshold Slope (SS) is an important figure of merit that can contribute to optimize standby power. For high speed applications a steeper subthreshold slope is desirable. SS primarily depends upon the carrier concentration in the subthreshold condition. Mathematical expression for SS is as follows [6][20][21]:

$$SS = \left[\frac{\partial log_{10}(I_D)}{[\partial V_{GS}]}\right]^{-1} \quad (4)$$

A plot of SS for both devices is indicated in Fig. 3(a).

From a low power design perspective another important parameter is the Drain Induced Barrier Lowering (DIBL). This effect in short channel devices occurs due to reduced energy barrier between the source and the channel, which causes an excess injection of charge carriers into the channel. It is also termed as the threshold voltage shift due to drain potential. Computing threshold voltage from constant drain current method, the value of DIBL is estimated by the equation [13][14][23].

$$DIBL\ (\frac{mV}{V}) = \frac{\Delta V_{th}}{\Delta V_D} \quad (5)$$

Transconductance generation factor TGF[21] is an analog performance parameter estimated by the equation

$$TGF = \frac{g_m}{I_D} \quad (6)$$

where $g_m = \frac{\partial I_D}{\partial V_G}$ is the transconductance of the device.

Device A exhibits a 10% improvement in TGF when compared to Device B. For drain to source voltage of 0.5V the transconductance in Device A has lower average trans-conductance (though of the same order), justifying the improved gate control.

In the case of low power design, another cause for concern in short channel devices is the leakage occurring with Gate Induced Drain Lowering (GIDL) [22][24]. GIDL is a phenomenon of band to band tunneling of charge carriers due to either high electric field, thinner oxides, lightly-doped drain regions and/or high V_{DD}.

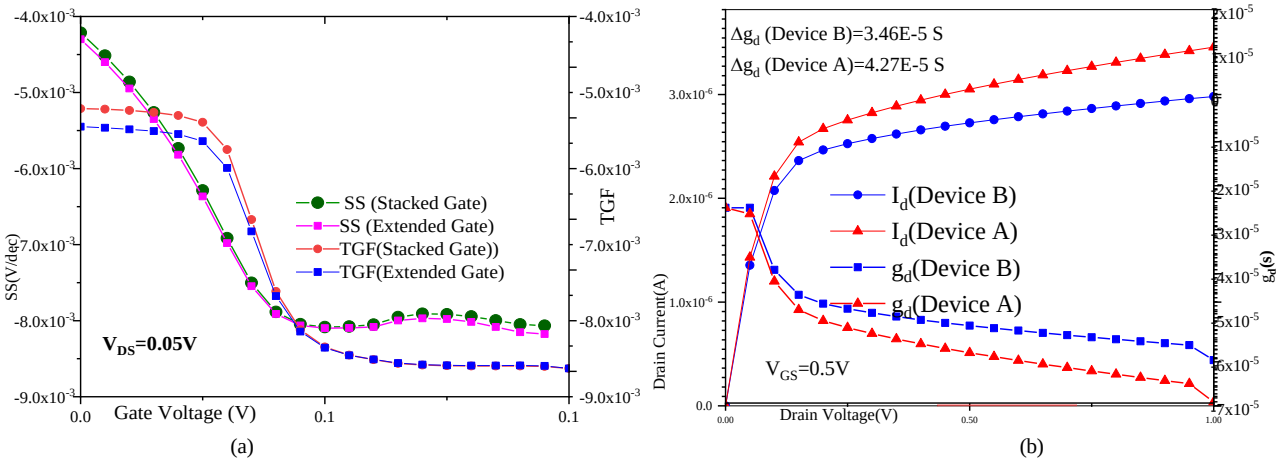


Fig. 3. (a) Subthreshold Slope (SS) and Transconductance Generation Factor (TGF) for Both Devices as Function of Gate Voltage for V_{DS}=0.05V (b) Drain Current and Output Drain-Conductance as a Function of V_{DS} for V_{GS}=0.5V.

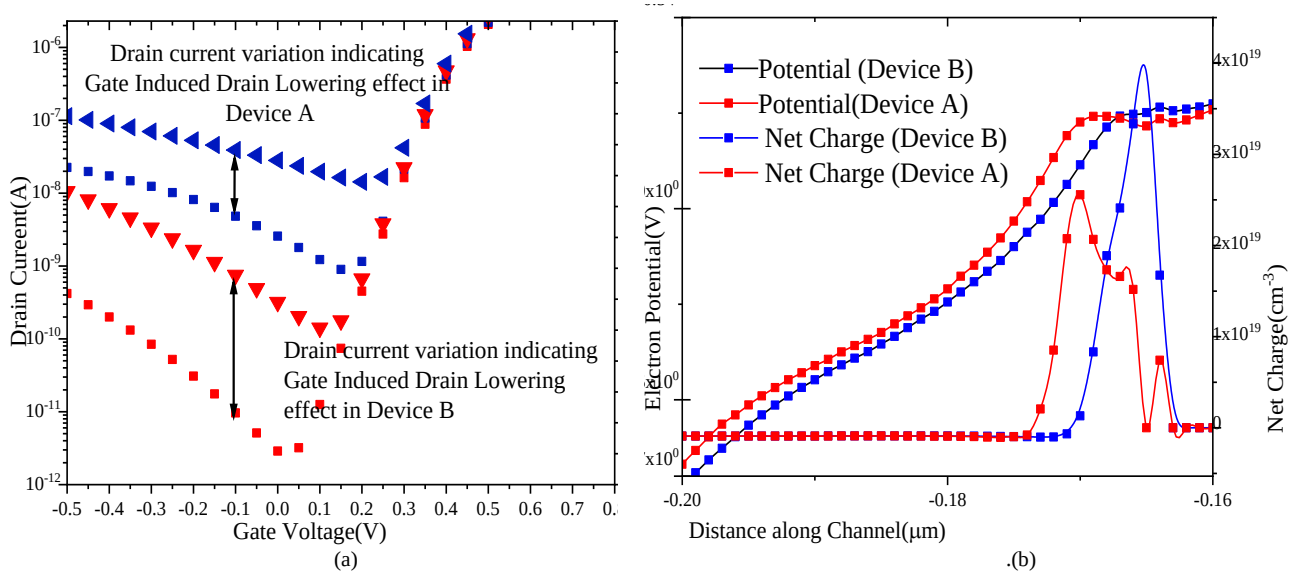


Fig. 4. (a) Gate Induced Drain Lowering Effect for Gate Voltage Variations. (b) Net Charge and Electron Potential Variation Along the Channel.

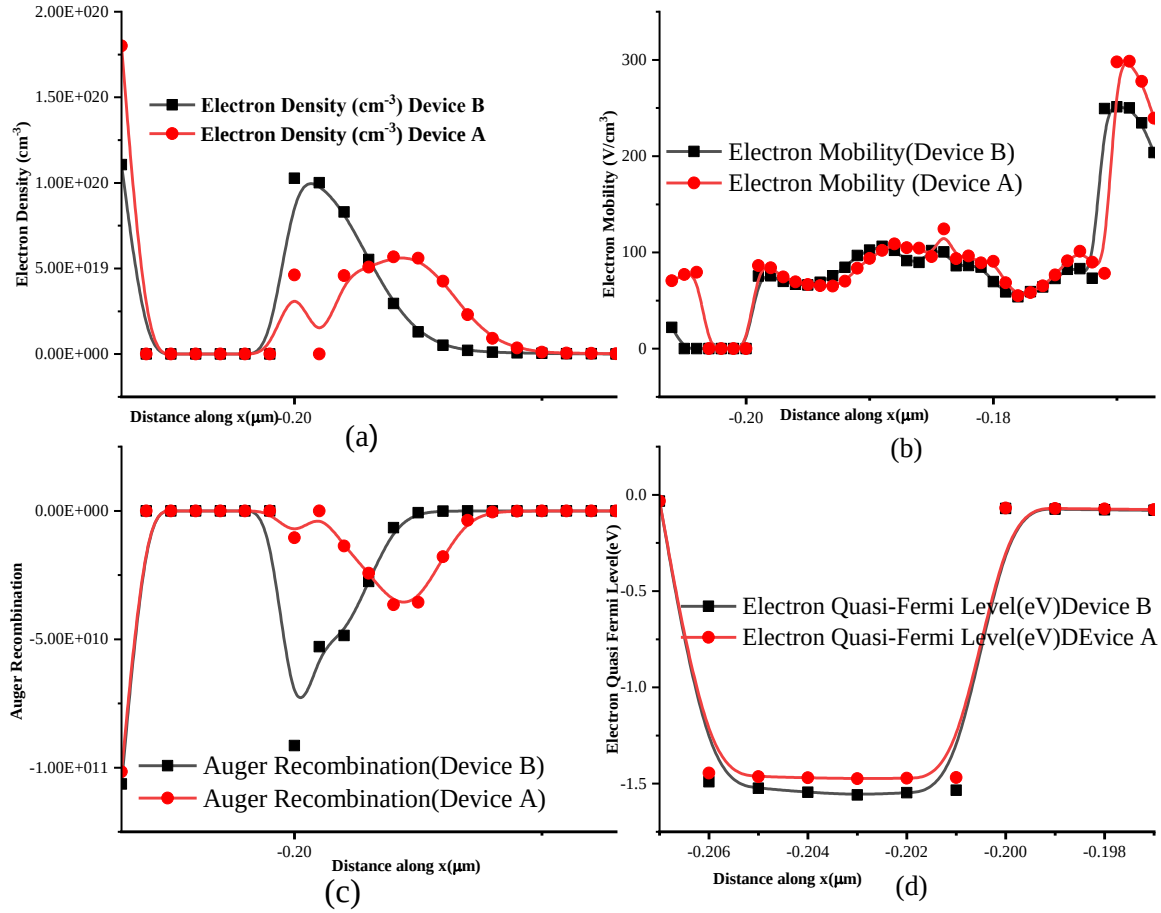


Fig. 5. Electrostatic Characteristics at V_{DS}=0.5V (a) Electron Density Along the Channel (b)Electron Mobility Along the Channel(c) Augur Recombination and (d) Electron Quasi Fermi Energy Level (eV) along the Channel in both Devices.

A plot of drain current against drain voltage and drain resistance is indicated for both devices in Fig. 3(b). Fig. 4(a) indicates the GIDL and (b) has net charge and electron potential variation along the channel for both the devices. Fig. 5 has plots of electron density, electron mobility, Auger recombination and electron quasi Fermi level along the channel for both the implemented devices.

III. Discussion on Simulation Results

On/Off current ratio: A plot of drain current (as shown in Fig. 2) indicates better on/off ratio in Device A as compared to Device B. There is a difference of 1.78 between the two values.

Transconductance: The average trans-conductance variation for V_{DS}=0.05 to V_{DS}=0.5V is $6.06x10^{-6}S$ in Device B. On the other hand, a variation of $4.48x10^{-6}S$ is observed in Device A. This is due to better control on the flow of charge carriers in the extended gate structure.

SS: SS as per Fig. 3(a) indicates improvement by 0.065mV/decade for Device A as compared to Device B, which is a desirable feature for faster switching applications.

Vth and TGF: Threshold voltages of both the devices are almost same but the change in TGF in Device A for two operating conditions (i.e. subthreshold region for V_{DS} =0.05V and saturation region for V_{DS}=0.5V) is observed to be 1.06 in comparison to 1.77 for Device B. Since power dissipation in subthreshold region is less, the impact on low power employability of the device may not get hampered.

g_d: The output drain conductance variation (referring to Fig. 3(b)) is also higher in Device A. The difference between the output drain conductance value lies in μS range which is very small. The metal gate stacking feature of both the implemented devices ensures uniform distribution of charges along the channel. For CMOS analog circuits it is desirable to have low value of drain transconductance that results in large value of drain current value for saturation region (amplifier) operation. Good control on channel means better control on channel length modulation and enhanced DIBL effect.

When both the devices are simulated for fixed V_{DS}=0.5V and gate voltage variation from –0.5 V to +0.8V, GIDL effect can be observed. As per the plot (Fig. 4(a)) there is almost a one order difference in the drain current values of both the devices.

The Figure of Merit (FOM) for describing leakage behavior in bulk devices proposed by [25] is given by

$$FOM = \frac{\Delta V_{(DIBLSS)}}{\left(I_{d,sat}/I_{sd,leak}\right)} \quad (7)$$

TABLE I. PERFORMANCE METRICS FOR DEVICE A AND B

Parameter	On-off Current Ratio	g_m		g_d	SS	V_{th}	TGF	
		V_{DS} (0.05V) S	V_{DS} (0.5V) S	S	mV/ decade	V	V_{DS} (0.05V) S/A	V_{DS} (0.5V) S/A
Stacked Gate FinFET(Device B)	3.43E+07	7.05444E-06	7.78277E-06	5.02E-05	7.49E+00	0.42	42.18	43.959
Stacked Gate FinFET with Gate Extension (Device A)	5.21E+07	3.79754E-05	4.04511E-05	5.63E-05	7.56E+01	0.42	39.31	40.36

The difference between the two FOM values though very small and of the same order, we can see that Device A has lesser value than Device B indicating improvement in leakage current control. The FOM values are 9.46E−14 and 1.71E−14 respectively.

There is also significant improvement in the net charge distribution as well as potential across the channel (seen in Fig. 4(b)). All the performance metric values are tabulated in Table 1.

The plot of electron density along the channel shows additional peak in device A with area under the curve almost same at 2.316E18 and 1.2874E18 for both Device A and Device B respectively.

Auger recombination: (Fig. 5(c)) Auger recombination involves three-carrier recombination process, either two electrons and one hole or two holes and one electron. In the active fin area this process is the major contributory factor that may lead to hot carrier injection thereby degrading performance. A plot of electron mobility along the channel shown in Fig. 5(b) exhibits higher mobility in Device A. An effective mobility enhancement of almost 30% is observed in Device A as compared to device B.

The quasi Fermi energy in the Device A has maximum difference of 0.847eV with respect to Device B (shown in Fig. 5(d)). The range of quasi Fermi level shows number of occupied energy states by the conducting electrons within the channel.

Internal Capacitances: Both the devices are simulated for extracting internal capacitive effects. This is achieved by applying DC voltage of 0.5V at the gate and drain terminals and AC signal of 0.001V at the gate. The values of gate to source and gate to drain capacitance extracted are in the range of 10^{-19}F. The capacitance values guarantee high frequency performance of the device up to Tera Hz range. The extracted average capacitance values are tabulated in Table 2.

TABLE II. INTRINSIC CAPACITANCES ESTIMATED FOR BOTH FINFET DEVICES

Capacitance F	C Gate-Substrate	C (Gate-Gate)	C (Gate-Source)	C (Gate-Drain)
Device B	7.34 E-022	1.08 E-017	7.06 E-019	7.24 E-019
Device A	4.58 E-024	1.10 E-017	7.16 E-019	7.17 E-019

IV. CONCLUSION

After evaluating performance metrics of both the FinFET devices it can be concluded that at the expense of the additional processing cost, a significant improvement in terms of leakage performance can be achieved with the new design. This conclusion is drawn from difference in FOM value by 7.75 E−14, steeper subthreshold slope (0.06mV/decade), improvement in mobility by 30%, and lowering of potential along the channel by 0. 035mV. This performance enhancement is an outcome of effective gate control.

The other parameters indicating performance improvement include uniform net charge distribution along the channel having value in the range of E18 cm^{-3}, and significant improvement in GIDL,

With internal capacitances in the $10^{-17}F$ range it is evident that the analog operating frequency range of the device is well above hundred TilGHz.

However, there is no significant improvement in the values of DIBL, output drain conductance, and threshold voltage. With available enhancement features this newly implemented device can further be optimized incorporating other techniques of metal work function engineering to explore their employability in low power applications. The property of higher on/off drain current ratio can be exploited for adopting a reduced voltage swing approach in low power VLSI design. Either by using them independently, in combination for circuit design, or by exploring the gate extension property further, a multi-threshold approach can also be used for low power VLSI design.

Finally, these devices can also provide a good solution for solving scaling related issues in short channel devices.

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