Low Power and High Reliable Triple Modular Redundancy Latch for Single and Multi-node Upset Mitigation

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***Abstract*—CMOS based circuits are more susceptible to the radiation environment as the critical charge (Q_{crit}) decreases with technology scaling. A single ionizing radiation particle is more likely to upset the sensitive nodes of the circuit and causes Single Event Upset (SEU). Subsequently, hardening latches to transient faults at control inputs due to either single or multi-nodes is progressively important. This paper proposes a Fully Robust Triple Modular Redundancy (FRTMR) latch. In FRTMR latch, a novel majority voter circuit is proposed with a minimum number of sensitive nodes. It is highly immune to single and multi-node upsets. The proposed latch is implemented using CMOS 45 nm process and is simulated in cadence spectre environment. Results demonstrate that the proposed latch achieves 17.83 % low power and 13.88 % low area compared to existing Triple Modular Redundant (TMR) latch. The current induced due to transient fault occurrence at various sensitive nodes are exhibited with a double exponential current source for circuit simulation with a minimum threshold current value of 40 µA.**

Keywords*—Multiple Event Transient (MET); Single Event Upset (SEU); Single Event Transient (SET); Radiation hardening; Reliability; Transient fault; Triple Modular Redundancy (TMR)

I. INTRODUCTION

The reliability issues are a major concern in semiconductor ICs designed for medical, space and defense applications that operate in a high radiation environment. As the CMOS technology scaling down, the supply voltage and node capacitance scales down as well. When high energy neutron or alpha particles passes through the MOS device, it causes an additional charge (excess electron-hole pair) induced in the substrate [1]. In specific, the sensitive node is the drain terminal of the OFF transistor. The induced additional charge collects by the drain terminal and turns on the device, causing in a voltage transient (or glitch) at the output. These glitches are called transient faults and are temporary in nature. Modelling the effect of transient fault on both NMOS and PMOS is shown in Fig. 1. To model the impact on NMOS transistor the double exponential current source is connected between the drain and source terminals of NMOS transistor as shown in Fig. 1(a). If the transient fault occurs on the drain terminal of NMOS transistor, a negative current spike is generated [22]. If the input gate voltage, $V_G = 0$ at that moment, V_{GD} becomes greater than the threshold voltage (V_{TN}), i.e. $V_{GD} > V_{TN}$ which runs the transistor in triode region. The output node then pulls down to logic 0.

To model the impact on PMOS transistor, the double exponential current source is connected as shown in Fig. 1(b). If the transient fault occurs on the drain terminal of PMOS transistor, positive current spike is generated. As a result the output node pulls up to logic 1. The output node recovers by removal of the current source [2]–[4]. If this transient pulse is propagated through memory element then, the Single Event Upset (SEU) occurs.

To evade these radiation effects, many hardened by design techniques have been proposed to deal with Single Event Transients (SETs), SEUs and Multiple Event Transients (METs) [5]–[21]. The advantages of these methods are that they are highly resistant to SETs and SEUs. The cost in terms of power dissipation, delay and area consumption for protecting memory elements from an SEU is substantial. SETs and SEUs are more general observed errors whereas, METs may occur due to packing density or single event triggering multiple transients.

This paper suggests a low power, less area and fully robust triple modular redundancy latch design (named as FRTMR) latch. The suggested latch is less sensitive to SEU and Multiple Event Upsets (MEU). The FRTMR latch comprises of three identical latch structures and a novel majority voter circuit. The three identical latch structures consist of six feedback loops (three of them will be active when the output of inverters INV1, INV2 and INV3 are 0 and the other three will be active when the output is 1). This saves power dissipation. The majority voter circuit designed with less number of transistors and less sensitive nodes compared to the existing classical TMR latch used in [12]. With less number of sensitive nodes, the probability of affecting the circuit due to transient faults is also less. FRTMR consumes considerably low power and less area than the existing classical TMR latch because of the less number of transistors used in majority voter circuit. Detailed analysis of FRTMR latch is presented in Section III.

The remaining sections of the paper are organized as follows: Section II discussed about some existing hardened latches. Section III describes the implementation, detailed analysis of proposed FRTMR latch with and without transient faults. Performance comparisons with existing latch are reported in Section IV. Section V concludes the paper.

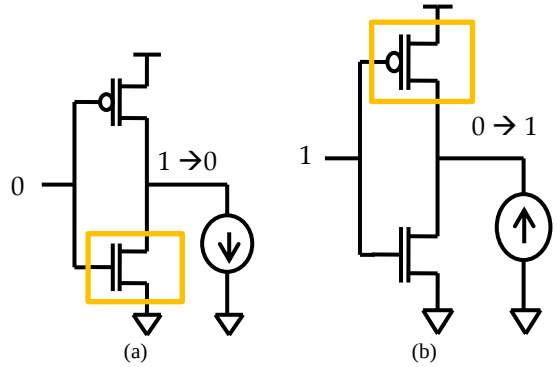

Fig. 1. Transient Fault Current Model on: (a) NMOS; (b) PMOS.

II. Related Work

Fig. 2 shows the conventional D-latch. This latch cannot function properly in highly radiated environments. During the latch mode, if a high energy particle strikes on the intermediates nodes n1 or n2. It may disrupt the state of the latch. This results in a wrong value at the output. To overcome this problem, many radiation-hardening latches have been proposed in the literatures.

Fig. 3 presents the circuit of the LCHR latch in [7]. The latch includes three redundant information retention feedback loops, which allows SEU to be tolerated in hold mode. The latch is capable of filtering single event transients arrived at input due to hysteresis property of Schmitt trigger (ST) inverter. Nevertheless, this circuit has following disadvantages: 1) in hold mode, there is a possible current competition, because the result is driven by a feedback loop and a C-element. This leads to more power dissipation. 2) Not economical because of area overhead and power dissipation. 3) Not completely self-recoverable from SEUs like DICE latch.

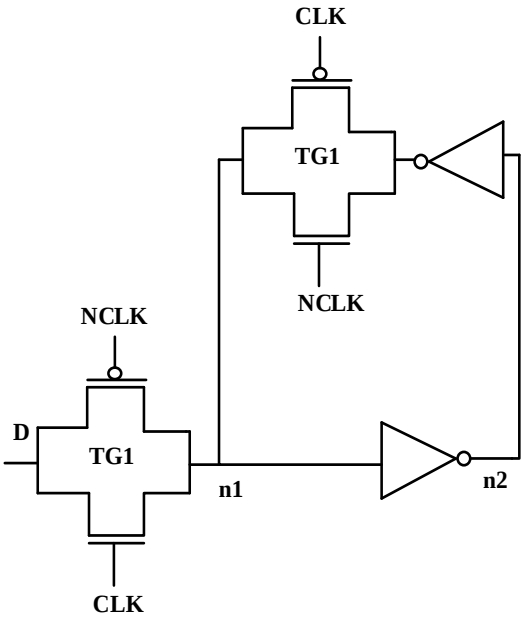

Fig. 2. Conventional Latch Structure.

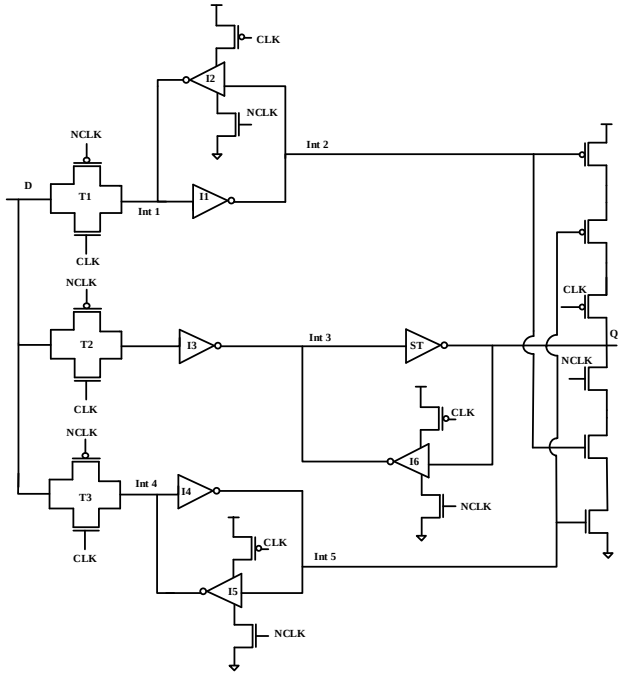

Fig. 3. LCHR Latch in [7].

The SEU resilient and SET filterable latch (RFEL) in [8] is presented in Fig. 4. This latch also includes three redundant information retention feedback loops in order to handle single node upsets due to particle strikes. The circuit uses a ST inverter in order to filter SETs in transparent mode of operation. But, the ST inverters cannot tolerate high energy particle strikes.

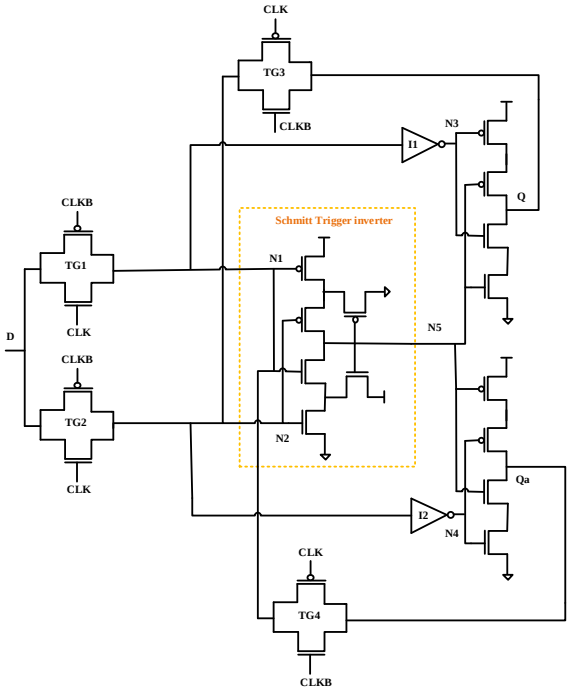

Fig. 4. RFEL Latch in [8].

Fig. 5 illustrates the latch circuit in [9]. The latch comprises of two interconnected structures. These cross-coupled structures form a negative feedback path. Feedback path for the latch are cut-off in transparent mode to improve the performance in terms of speed. In the latch mode, feedback structure enables to restore temporary failures because of SEUs. However, it cannot tolerate high energy particle strikes, and also consumes large silicon area.

The latch design in [10] is shown in Fig. 6. It comprises of a static D-latch and an error detection circuit. Error detection circuit plays a major role in mitigating soft errors. However, if the transient fault occurs on error detection circuit, it produces an erroneous value. Also, it has an extensive area overhead and power dissipation.

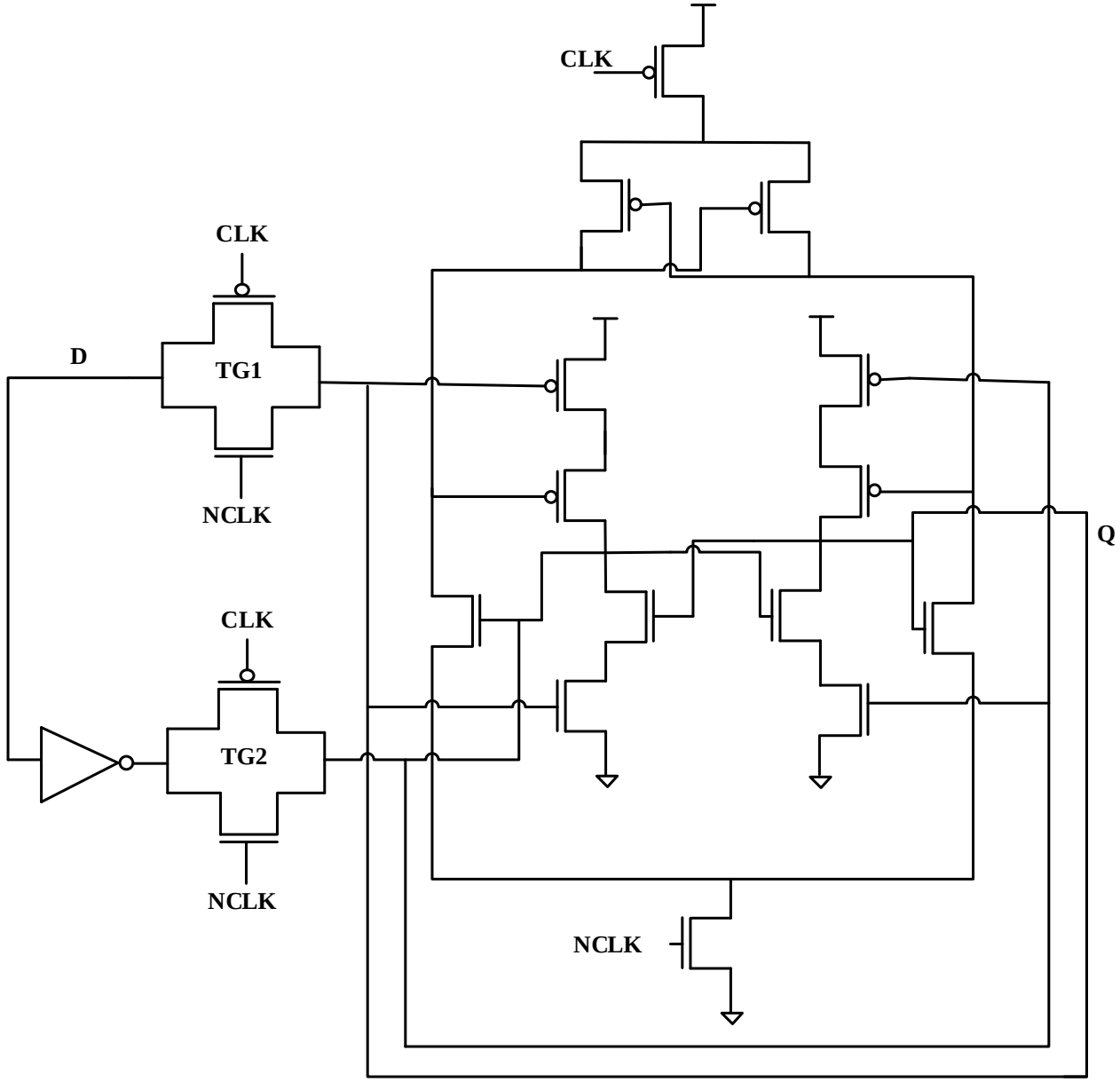

Fig. 5. Latch in [9].

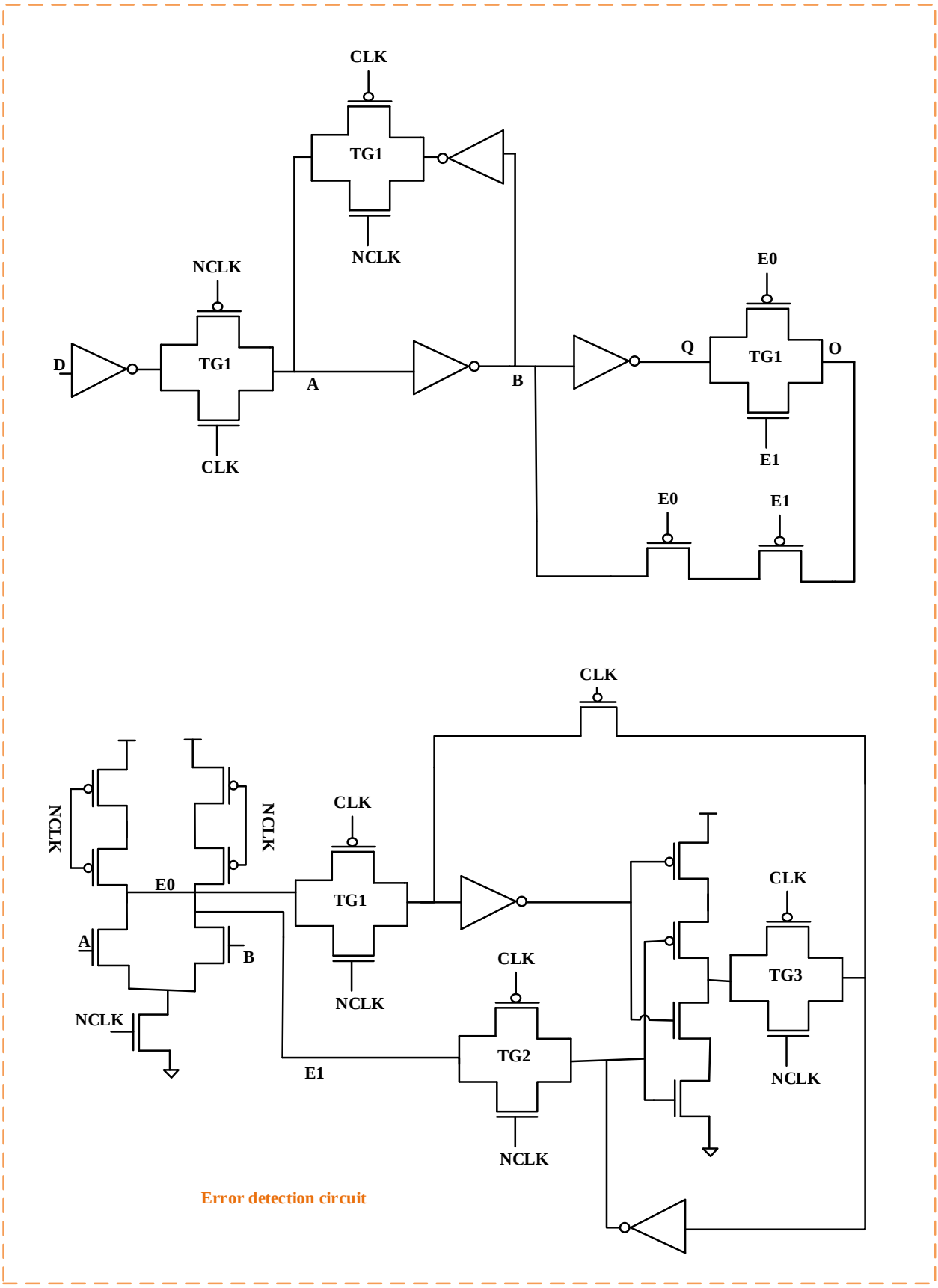

Fig. 6. Latch in [10].

The latch designed in [11] is shown in Fig. 7. It consists of three transmission gates, a memory element and a clocked Muller C-element to save power dissipation. Nonetheless, it cannot tolerate multi-node upsets and also if the transient fault occurs on intermediate nodes of C-element it produces a glitch at the output. SEU tolerant latches to mitigate the single event upsets also include DICE, Quatro [20] and TMR latch used in [12, 13]. All the above discussed latches are not multi-node upset tolerant.

The classical TMR latch is presented in Fig. 8. It consists of three identical latch circuits which individually perform the same operation and these results are processed by a majority voter circuit to produce a solitary output. It can tolerate SEU occurring on any one of the three identical latches, as long as the other two inputs continue to be stable, and provide 100% SEU immunity on the internal nodes N1 (or A), N2 (or B) and N3 (or C). In this paper these nodes are signified as "self-recoverable" (SR) nodes as the output can be self-recovered from any type of single node upsets. Nevertheless, an SET on the internal nodes (n1 – n5) of a voter circuit can cause a voltage transient at the output. These nodes are named as "critical nodes" (CN) as the output can't be recovered themselves until and unless the transient pulse is removed from the critical nodes.

Though, TMR latch is most prevalent hardened technique used in aerospace applications for its high reliability, many researchers tend to develop radiation hardened latch designs using the following techniques: 1) ST inverter. 2) Muller C-element. 3) DICE principle. 4) Error correction mechanism. The primary reason is that it incurs huge area and power dissipation. Also, the number of critical nodes is more. In addition to this, the existing TMR latch is not suitable for multi- node upsets. Our proposed FRTMR latch in section III resolves these issues properly.

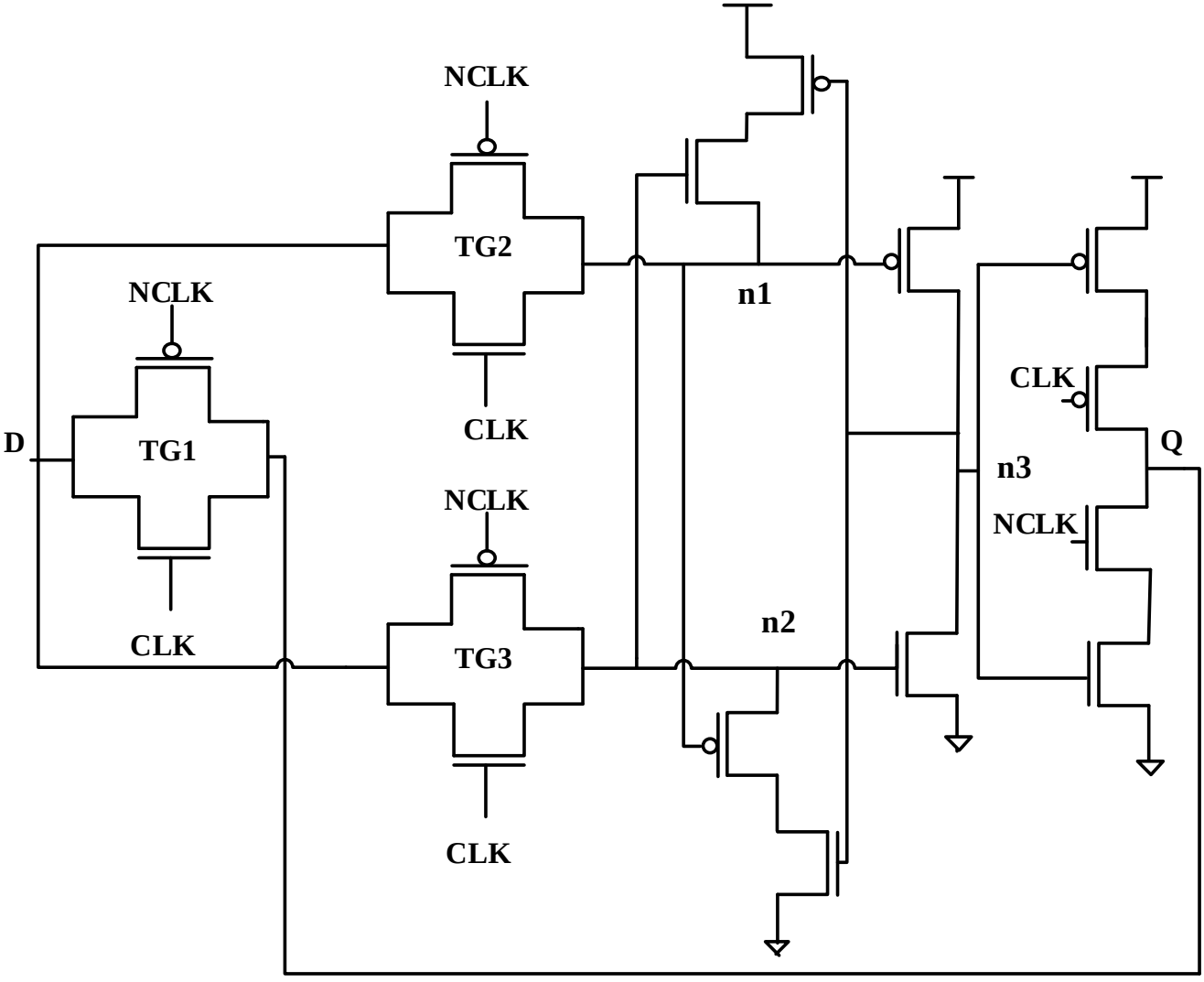

Fig. 7. Latch in [11].

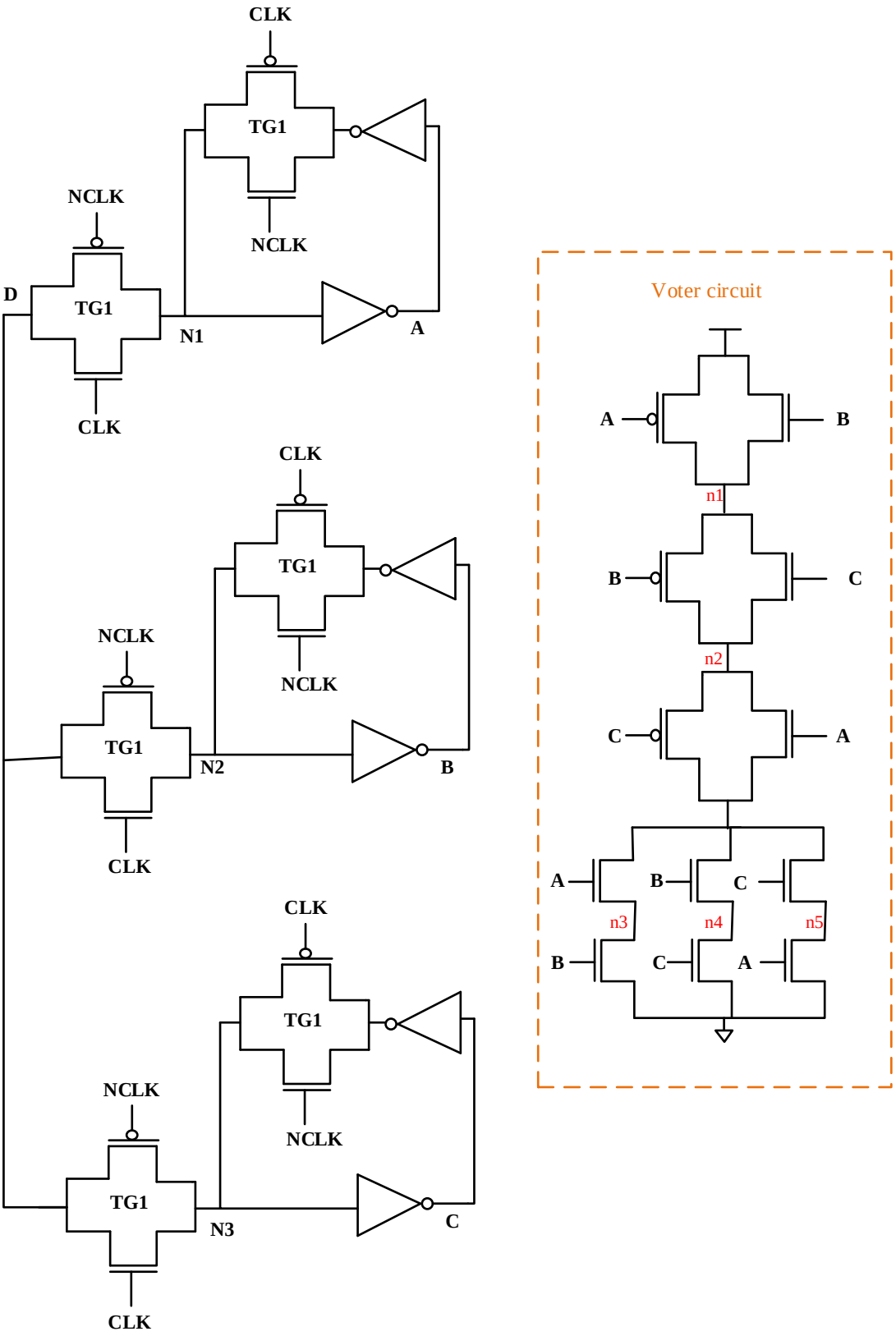

Fig. 8. Classical TMR Latch.

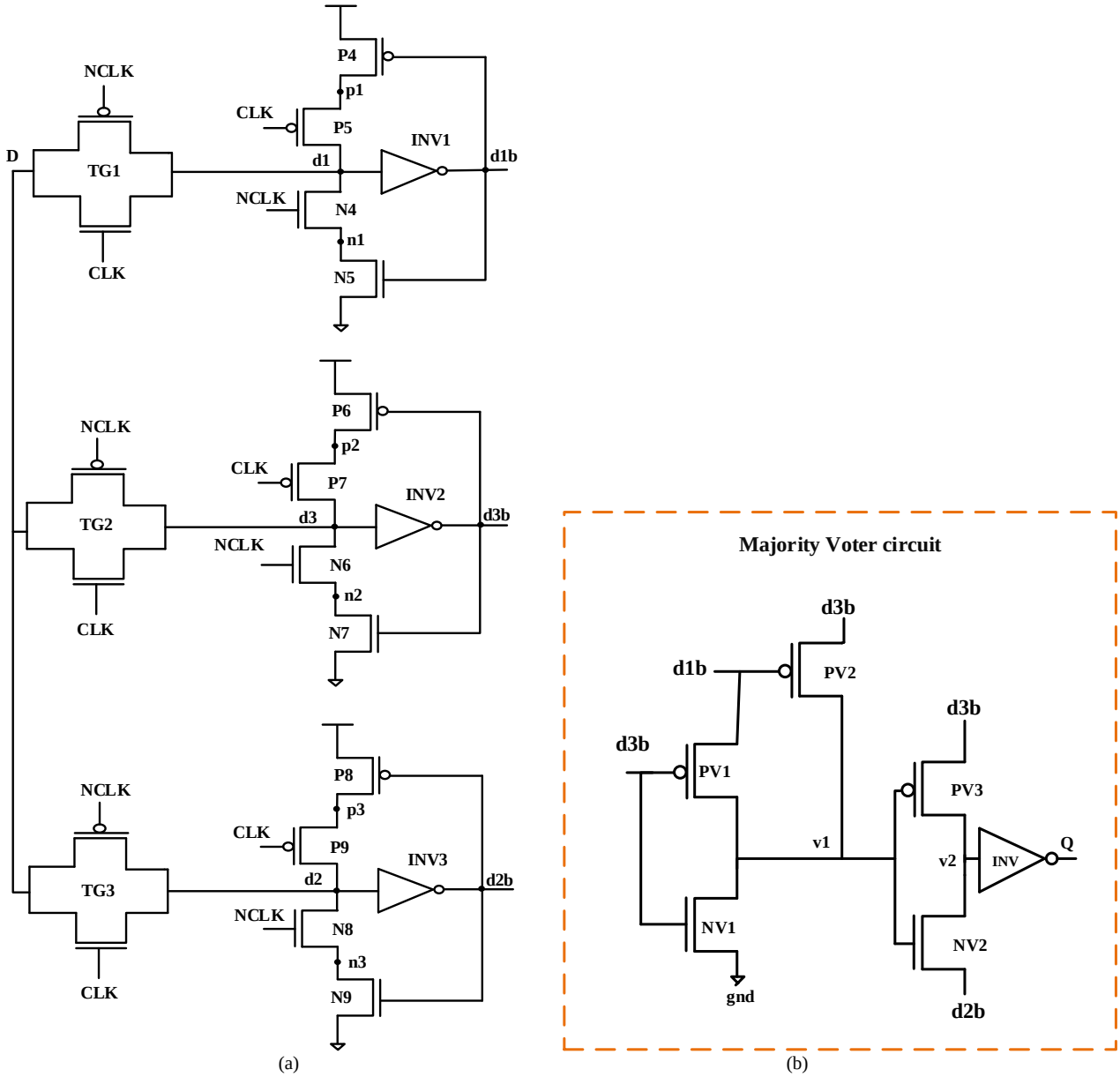

Fig. 9. Proposed FRTMR Latch: (a) Three Identical Latch Configurations; (b) Majority Voter Circuit.

III. Proposed FRTMR Hardened Latch

The proposed FRTMR latch is shown in Fig. 9. From Fig. 9, it can be observed that the three identical latch circuits shown in Fig. 9(a) perform the operation and the results are processed by a majority voter circuit shown in Fig. 9(b) to produce a solitary output. According to Fig. 9, D, Q, CLK and NCLK are input, output, system clock and system negative clock respectively.

During transparent mode (when CLK = 1 & NCLK = 0) the transmission gates (TG1 – TG3) are ON. For D = 0, (i.e., d1 = d3 = d2 = 0) the PMOS transistors of INV1 – INV3 are ON which results in d1b = d3b = b2b = 1 and subsequently, these values are fed to majority voter circuit. In the majority voter circuit for d1b = d3b = d2b = 1, transistors PV1 and PV2 are OFF, NV1 is ON and hence, V1 = 0. Consequently, node v2 = 1 through PV3 transistor. This v2 node voltage propagates through inverter (INV) and produces the output Q = 0.

For D = 1, (i.e., d1 = d3 = d2 = 1) the NMOS transistors of INV1 – INV3 are ON which results in d1b = d3b = d2b = 0 and subsequently, these values are fed to majority voter circuit and makes v1= 0. As a result, node v2 = 0 and hence, output Q = 1.

During latch mode (when CLK = 0 & NCLK =1) the transmission gates (TG1 – TG3) are OFF, and hence, the internal nodes retain their current values through the NMOS transistors of feedback loops for D = 0 and PMOS transistors of feedback loops for D = 1. As a result, the latch outputs the correct value in the latch mode.

Now, the detailed working of FRTMR latch in the presence of transient fault at various internal nodes (d1, d3, d2, d1b, d3b, d2b, v1 and v2) is explained in this section. Note that, the

storage of 0 of the latch is considered for all fault-tolerance discussions throughout the paper. In normal operation (without transient fault) for data input D = 0 case, d1 = d3 = d2 = v1 = Q = 0 and d1b = d3b = d2b = v2 = 1. In general, SET is analyzed only in latch mode.

SET on node d1: In this case, d1 flips its state from 0 → 1, and the corresponding node d1b changes its state from 1 → 0. Therefore, the node voltages at d1b, d3b and d2b are 0, 1 and 1 respectively. These values are fed to majority voter circuit. In the majority voter circuit for d1b = 0 and d3b = d2b =1, transistor PV1 is OFF, PV2 and NV1 are ON simultaneously. In order to perform the latch operation correctly, PV2 transistor in the majority voter circuit shown in Fig. 9(b) is sized 10 times (i.e., W/L = 1500 nm/45 nm) faster than NV1 (i.e., W/L = 150 nm/45 nm). The sizing of these transistors helps in maintaining the value of v1 at logic 1. As a result, the node v2 becomes 1. This v2 node voltage drives the inverter (INV) and produces the correct output. The voltage levels at node v1 for various W/L ratios of PV2 and NV1 for different combinations of d1b, d3b and d2b are shown in Fig. 10.

SET on node d3: In this case, d3 flips its state from 0 → 1, and the corresponding node d3b changes its state from 1 → 0. Therefore, the node voltages at d1b, d3b and d2b are 1, 0 and 1 respectively. These values are fed to majority voter circuit. In the majority voter circuit for d3b = 0 and d1b = d2b =1, transistors NV1 and PV2 are OFF, PV1 is ON and hence, v1= 1 and successively, v2 = 1. This v2 node voltage is propagated through inverter (INV) to produce the correct output.

SET on node d2: In this case, d2 flips its state from 0 → 1, and the corresponding node d2b changes its state from 1 → 0. Therefore, the node voltages at d1b, d3b and d2b are 1, 1 and 0 respectively. These values are fed to majority voter circuit. In the majority voter circuit for d2b = 0 and d1b = d3b =1, transistors PV1 and PV2 are OFF, NV1 is ON and hence v1 = 0 and successively, v2 = 1 through PV3 transistor. This v2 node voltage is propagated through inverter (INV) to produce the correct output. The analysis is same for d1b, d3b and d2b.

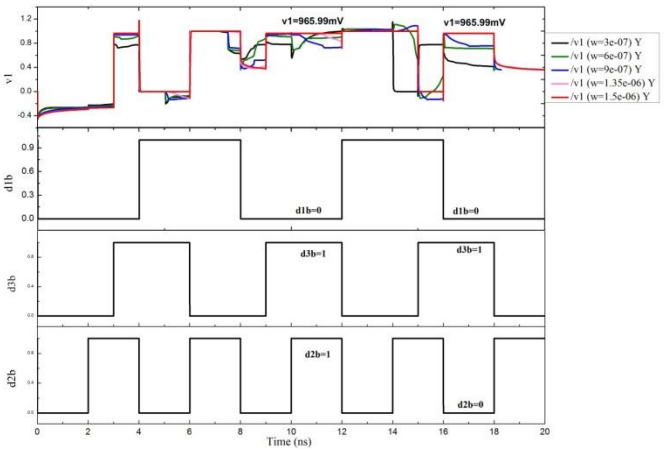

Fig. 10. Parametric Analysis to Determine the width of the Transistors W_{PV2} /W_{NV1}..

SET on node v1: Without transient fault for D = 0, d1 = d3 = d2 = 0, d1b = d3b = d2b =1, and the internal node v1 and v2 are 0 and 1 respectively. Now, If transient fault occurs on node v1, it flips its state from 0 → 1. Subsequently, node v2 becomes 1. This v2 node voltage drives the inverter (INV) and produces the correct output.

SET on node v2: If the transient fault occurs at node v2, it produces glitch at the output immediately and remains until the transient fault effect presents at the node. The output will be recovered after the transient fault dies down. In the proposed latch, internal nodes d1, d3, d2, d1b, d3b, d2b and v1 are termed as "self-recoverable" nodes and v2 as "critical node".

Fig. 11 shows the simulation results of FRTMR latch for without and with transient fault injections (highlighted in the Fig. 11) on internal nodes d1, d3, d2, d1b, d3b and d2b at different time periods. The minimum threshold current value imposed on the internal nodes is 40 μA. Similarly, Fig. 12 shows the simulation results of FRTMR latch with transient fault injections on nodes v1 and v2 at different time periods. The minimum threshold current value applied to these nodes is 60 μA. From Fig. 11 and Fig. 12, it can be observed that transient fault at any internal node (except v2) can be 100% tolerable since the output node Q constantly remains at correct value. In case of node v2, the output produces glitch and the glitch remains until the transient fault dies down.

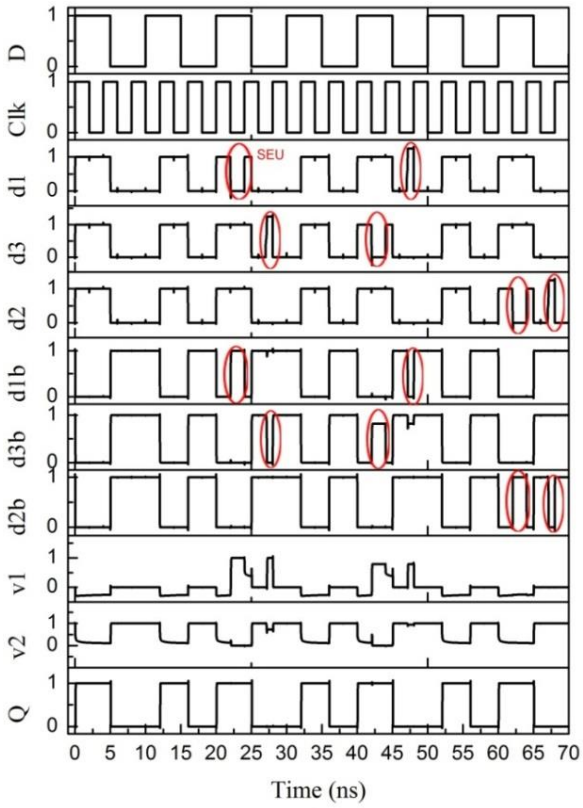

Fig. 11. Simulation Results of FRTMR latch without and with Transient Fault Injections at d1, d3, d2 for D = 0 & 1.

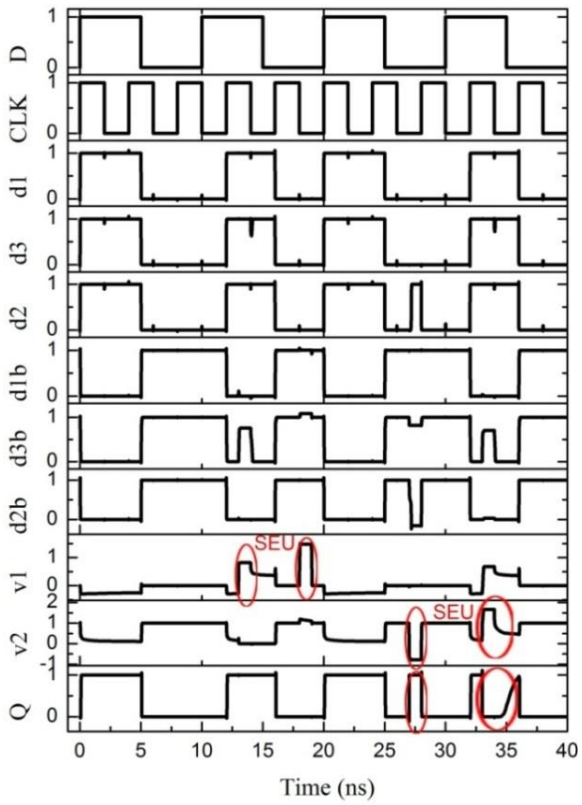

Fig. 12. Simulation Results of FRTMR latch with Transient Fault Injections at v1 and v2 for D = 0 and 1.

From Fig. 11 and Fig. 12, statistics results for the SETs at internal nodes of FRTMR latch design are extracted and presented in Table I. According to Table I, for D = 1, transient fault is injected at 22 ns on node d1. It can be observed that the change in node voltage from 1 → 0, changes d1b from 0 → 1. Although, the output remains correct. Likewise, it is true for the other cases too. Table I also shows the statistics results for D = 1. From the Table I it can be observed that result "SR" denotes as "self-recoverable" nodes, where the output can completely self-recovered from any single node transient injection. Similarly "CN" as "critical nodes" where these nodes can flip the output node voltage and remains until the transient fault injection is removed from that node.

The detailed behaviour of FRTMR latch at internal nodes (d1, d3, d2, d1b, d3b, d2b, v1 and v2) for the data inputs D = 0 & 1 is presented in Table II. Transient fault occurrence to the nodes is highlighted in the table.

A. Multiple Event Transient Analysis of FRTMR Latch

This section elaborates the multi-node upset tolerance analysis of the FRTMR latch. Multiple Event Transients (METs) may occur due to packing density or single events cause multiple transients. However, TMR circuits are only immune to SETs that effect to a single redundancy. Multiple SETs that affect multiple redundancies causes functional failure. Our definition of multi-node in this paper is a node on any one of the redundant latch and node v1 of voter circuit. Node v2 is not considering for multi node upsets as this is a critical node.

MET on <d1, v1>: d1 flip from 0 → 1 and d1b from 1 → 0, the nMOS transistor NV1 is ON and hence v1= 0. On the other hand, since v1 is also affected by transient fault simultaneously, it becomes 1. Thus, v2 = 1. Hence, output Q retains its correct value i.e., Q = 0.

MET on <d3, v1>: d3 flip from 0 → 1 and d3b from 1 → 0, the pMOS transistor PV1 is ON and hence, v1= 1. On the other hand, due to transient fault at v1simultaneously, v1 also tries to become 1. This makes v2 = 1. Hence, output Q retains its correct value i.e., Q = 0.

MET on <d2, v1>: d2 flip from 0 → 1 and d2b from 1 → 0, the nMOS transistor NV1 is ON and hence, v1 = 0. But, due to transient fault at v1, it becomes 1 straight away. This makes v2 = 0. Resulting a wrong data stored at the output i.e., Q = 1. As discussed in the section II, this pair of node is treated as critical node.

Similarly, in the case of 1 being stored, it can be found through an examination that the MET on <d1, v1> and <d1, v1> are 100% self-recoverable, whereas MET on <d2, v1> produces the wrong output. Fig. 13 shows the simulation results of METs of FRTMR latch for data inputs 0 and 1. From Fig. 13, statistics results for the METs at internal node pairs discussed above of FRTMR latch design are extracted and presented in Table III.

TABLE. I. STATISTICS RESULTS OF SET INJECTION OF FRTMRLATCH BASED ON FIG. 11 & 12 (FOR D = 1 & 0)

Time (ns)	Node	(D = 1) Output	Result	Time (ns)	Node	(D = 0) Output	Result
22	d1	Q = 1	SR	47	d1	Q = 0	SR
42	d3	Q = 1	SR	27	d3	Q = 0	SR
62	d2	Q = 1	SR	67	d2	Q = 0	SR
73	v1	Q = 1	SR	93	v1	Q = 0	SR
87	v2	Q = 0	CN	97	v2	Q = 1	CN

TABLE. II. SEU ANALYSIS ON INTERNAL NODES WITH DATA INPUT (D = 0 & 1)

Input (D)	d1	d3	d2	d1b	d3b	d2b	v1	v2	Output (Q)
0	0	0	0	1	1	1	0	1	0 (without SEU)
0	**1**	0	0	0	1	1	1	1	√
0	0	**1**	0	1	0	1	1	1	√
0	0	0	**1**	1	1	0	0	1	√
0	0	0	0	1	1	1	**1**	1	√
0	0	0	0	1	1	1	0	**0**	×
1	1	1	1	0	0	0	0	0	1 (without SEU)
1	**0**	1	1	1	0	0	1	0	√
1	1	**0**	1	0	1	0	1	0	√
1	1	1	**0**	0	0	1	0	0	√
1	1	1	1	0	1	0	**1**	0	√
1	1	1	0	0	0	0	0	**1**	×

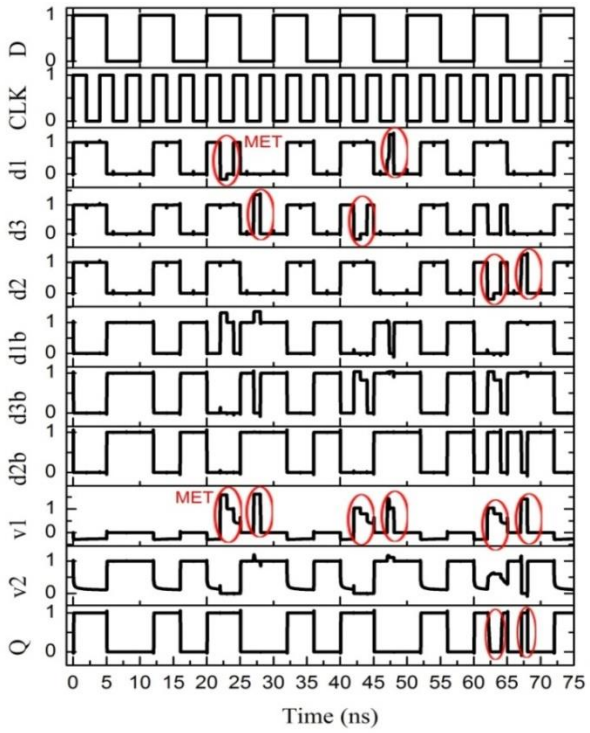

Fig. 13. Simulation Results of MET Injections of the FRTMR Latch for D=0 and 1.

TABLE. III. STATISTICS RESULTS OF MET INJECTION OF FRTMR LATCH BASED ON FIG. 13 (FOR D = 1 & 0)

Time (ns)	Node	Output (D = 1)	Result	Time (ns)	Node	Output (D=0)	Result
22	<d1,v1>	Q = 1	SR	47	<d1,v1>	Q = 0	SR
42	<d3,v1>	Q = 1	SR	27	<d3,v1>	Q = 0	SR
62	<d2,v1>	Q = 0	CN	67	<d2,v1>	Q = 1	CN

SR=Self Recoverable; CN=Critical Node

B. Novel Majority Voter Circuit

Majority voter circuit plays a vital role in TMR design. In TMR circuits, voter circuits are placed around redundant latches to continuously monitor the three logic redundancies. When an SET occurs on any one of the three redundancies, these voter circuits prevent the latches from permanent failure of the logic. The output expression of a transistor level majority voter circuit from Fig. 8 can be derived as:

$$((A \times B) + (B \times C) + (C \times A))' \quad (1)$$

As per the discussion in section II, the disadvantage of the majority voter circuit is, it has more number of critical nodes (n1-n5) i.e., 5 critical nodes. The critical nodes are inversely proportional to reliability. This paper proposes a novel majority voter circuit with only 2 internal nodes out of which, 1 is signified as self-recoverable node and the other is signified as critical node. Equation (2), (3) and (4) are derived at internal nodes v1, v2 and Q of majority voter circuit shown in Fig. 9(b).

$$V1 = d1b \oplus d3b \quad (2)$$

$$V2 = [(d1b \times d3b) + d2b(d1b \oplus d3b)] \quad (3)$$

$$Q = [(d1b \times d3b) + d2b(d1b \oplus d3b)]' \quad (4)$$

IV. PERFORMANCE EVALUATION AND COMPARISON

A classical TMR latch shown in Fig. 8 is considered as reference latch as this circuit is also used a voter circuit for hardening technique. To examine the performance of FRTMR latch, delay (D → Q), power, area, PDP and critical nodes are considered. For the purpose of comparison, the proposed FRTMR latch and existing latches, namely, LCHR, REFL, Latch in [9], [10], [11] and classical TMR Latch are implemented in 45 nm technology with the supply voltage of 1V and 250MHz clock frequency. The implemented latches are simulated in Cadence spectre environment. Table IV compares the evaluation costs for the FRTMR and existing latches with regard to delay, power, PDP, area, critical nodes, etc. From the Table IV, it may be noted that the power consumption of FRTMR latch is 85%, 44.3%, 88% and 17.83% reduced compared to LCHR, Latch in [9], Latch in [10] and classical TMR latch. And also it is third lowest compared with the latches reported in the Table IV. FRTMR latch has 13.8%, 18.4% and 13.88% reduction in area when compared to LCHR, Latch in [10] and classical TMR latch. But it has a trade-off in delay compared to reference latch. It is only best to LCHR latch. Nevertheless, FRTMR latch is more robust for SETs because of the less number of critical nodes (only 1). The proposed FRTMR latch can tolerate multi-node upsets compared to all the latches reported in Table IV.

TABLE. IV. PERFORMANCE COMPARISONS

	Delay (ps)	Power (nW)	PDP (fJ)	Area (# of transistors)	# of Critical nodes	MET tolerant (Yes/ No)
LCHR in [7]	118.7	4880	580	36	7	No
REFL in [8]	67	490	33	26	7	No
Latch in [9]	26.38	1273	33.6	20	-	No
Latch in [10]	73	6077	444	38	11	No
Latch in [11]	3.99	211.3	0.841	16	2	No
Classical TMR latch	48.16	863	41.6	36	5	No
FRTMR latch	66.76	709.09	47.34	31	1	Yes

V. CONCLUSION

At deep sub-micron technology, the CMOS integrated circuits are more likely to experience the occurrence of SETs and METs. This paper proposed FRTMR latch with novel majority voter circuit in 45 nm technology which can tolerate single and multi-node upsets. Generally, the TMR structures consume large silicon area and high power consumption. But,

the proposed FRTMR latch offers, low power and less area i.e. 17.83% and 13.88% respectively compared to existing classical TMR latch. The simulation results demonstrate that the FRTMR latch has 80% improved SEU tolerance than the classical TMR latch. Nonetheless, it has a tradeoff in delay i.e., 38.6% more delay compared to classical TMR latch.

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