Design and Analysis of an Arithmetic and Logic Unit using Single Electron Transistor

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***Abstract*—The demand for low power dissipation and increasing speed elicits numerous research efforts in the field of nano CMOS technology. The Arithmetic Logic Unit is the core of any central processing unit. In this paper, we designed a 4-bit Arithmetic and Logic Unit (ALU) using Single Electron Transistor (SET). Single-electron transistor (SET) is a new type of switching nanodevice that uses controlled single-electron tunneling to amplify the current. The single-electron transistor (SET) is highly scalable and possesses ultra-low power consumption when compared to conventional semiconductor devices. Reversible logic gates designed using SET are used for performing 4-bit arithmetic operations. We modelled symmetric single gate SET operating at room temperature using Verilog A code. The design is carried out in cadence simulation environment. The 4-bit SET based ALU design exhibits the power of 0.52 nW and delay of 350pS.**

***Keywords*—Single electron transistor; reversible logic gates; low power; speed**

I. Introduction

Miniaturization has brought electronic devices close to the size where quantum phenomena play a significant role in altering the whole device properties. Nano-scale devices like Single Electron Transistor (SET), Resonance Tunneling Diode (RTD), Quantum Cellular Automata (QCA) and Carbon Nano Tube (CNT) can often perform the same tasks similar to microscale devices such as Field Effect Transistors, yet the working principles are different. The single-electron transistor (SET) is one of the fascinating nanodevices. SET can perform as a switch and exploits the quantum mechanical phenomenon of electron tunneling through the tunnel junctions and also control the transport of single electrons [1,2]. The different models used for simulation of SET are as follows: Uchida's model [3] is more feasible at higher temperatures and over a huge range of drain voltages. The MIB model [4] is more flexible than Uchida's model and fewer exponential terms exist, so simulation time is lesser. Inokawa's model [5] is an extension of Uchida's model for asymmetric SETs in which the source and drain resistance, capacitance are unequal. A new computation model has been proposed to perform the arithmetic functions by controlling the movement of electrons within the circuit. Using this model, they designed 4-bit Digital to Analog Converter, adder, and multiplier circuits. The quantitative and qualitative comparison in terms of delay, sensitivity to process variations by varying the SET parameters, temperature, bias current and drain voltage of SET based circuits had been analyzed using SPICE, SIMON simulator. A novel quasi analytical model has been developed and validated for single-electron transistors based logic circuit simulation in static and dynamic regimes as well as for hybrid-SET by combining SET with MOSFET had been reported [6-15]. Sharifi.M.J et al. [18] proposed speed enhancement and bit error rate reduction in SET based digital circuits by reducing tunneling wait time.

An ALU is a combinational circuit that can perform a set of basic arithmetic and logical operations. Modern central processing unit (CPUs) and graphics processing units (GPUs) contain very dynamic and complex ALUs acting as the fundamental building block. Several research works had been proposed on reversible gate based ALU design. Reversible Logic plays a major role in fields such as Nanotechnology, low power CMOS design, optical computing, low loss computing. Limited research work was carried on SET based arithmetic circuits. In this paper, we used reversible gates using SET based on the MIB model for performing arithmetic operations. The Feynman gate is the most basic reversible gate. It is the only 2x2 reversible gate mainly used for fan-out purposes. The Toffoli gate, Fredkin gate, New gate and Peres gate are 3x3 reversible gates that can be used to realize various Boolean functions. The TSG gate, MKG gate, HNG gate, PFAG gate are 4x4 reversible gates that are designed to implement reversible adders. Slimani Ayyoub et al. [16] designed ALU using double Peres gate reversible logic to reduce quantum cost, the number of garbage outputs and depth of the circuits. Bolhassani, A et al. [17] developed new reversible ALU using elementary quantum gates which can be used in the implementation of Quantum computers. Vandana Shukla et al. [19,22] proposed a novel design approach for a 2-bit ALU design using 8:1 MUX with the reversible logic and simulated using Modelsim tool. Shahram Babaie et al. [20] designed Quantum cellular automata multilayer ALU to perform arithmetic and logical operation using QCA designer tool. Aarthy et al. [21] developed binary multiplier using single gate SET, double gate SET and hybrid SET by combining SET with MOSFET and analyzed the performance in terms of area, power and delay. The research paper is organized as follows: Section II describes the working principle and characteristics of SET. Section III describes the working model of SET based 4-bit ALU. The outcome of the proposed model has been elaborated in Section IV. Finally, the paper concludes in Section V.

II. SET Framework

The SET consists of a metallic island, placed between the source and drain tunnel junctions and has a gate electrode similar to regular FET. The tunnel junctions are thin (<10 nm)

oxide layer between the island and the gate electrodes. Quantum dots have been used as islands for the SET. Both tunnel junctions in the SET have intrinsic tunnel resistance (R_{ts} and R_{td}) and capacitance (C_{ts} and C_{td}) parallel to each other. The SET schematic is shown in Fig. 1.

The SET island is very small in the nanometric scale accommodating a vast number of electrons. We can add or subtract electrons from the island, either by charging it positively or negatively based on the electron tunneling. The number of excess electrons on the island is denoted as n. The value of n can also be negative, which means that electrons have been removed from the island, leaving a positive charge. The electrostatic energy of the system is affected by the presence of excess electrons, which depends on the charge of the island.

$$E_C = \frac{1}{2}\frac{Q_{island}^2}{C_\Sigma} = \frac{1}{2}\frac{n^2 e^2}{C_\Sigma} \quad (1)$$

Where Q_{island} is the charge on the island, n the number of excess electrons, e is the charge of an electron and C_Σ the total capacitance which is equal to

$$C_\Sigma = C_{g1} + C_{g2} + C_{ts} + C_{td} \quad (2)$$

where C_{g1}, C_{g2} are gate capacitance and C_{ts}, C_{td} are the intrinsic source and drain tunnel junction capacitance.

The electrostatic energy of the system becomes

$$E_{electrostatic} = \frac{1}{2}\frac{Q^2}{C_\Sigma} = \frac{1}{2}\frac{(ne-Q_g)^2}{C_\Sigma} = \frac{1}{2}\frac{(ne-V_g C_g)^2}{C_\Sigma} \quad (3)$$

Where Q_g is the gate charge. This energy determines if electron tunneling through a junction is restricted or allowed. The addition of an excess electron on the island increases the energy of the system, then electron tunneling will be energetically prohibited, so no tunneling occurs through the junction known as the Coulomb blockade. The drain-source potential V_{ds} determines the energy of the electrons before the junction. Only if this energy is greater than the Coulomb blockade, the electrons will overcome the blockade and tunneling will occur. Mainly, the Coulomb blockade is based on the number of excess electrons on the island (n) and the gate charge (C_g).

A. Parameters that Improve the Performance of SET

The single-electron transistor performance is not merely determined by source voltage (V_s), drain voltage (V_d) and gate voltage (V_g) but also by other parameters such as external charges and temperature. Increasing the charging energy ($\frac{e^2}{2C_\Sigma}$) in the SET will provide the possibility of SET to operate at high temperatures, which is obtained by reducing the device capacitance to a very small value (in the order of 10^{-18} F) since the electrostatic energy is inversely proportional to it ($E_C = \frac{Q^2}{C_\Sigma}$). The presence of charges that are not on the SET island but nearby referred to as external charges' is one more important parameter that can cause a severe problem like an uncontrolled drift of threshold voltage of the transistors.

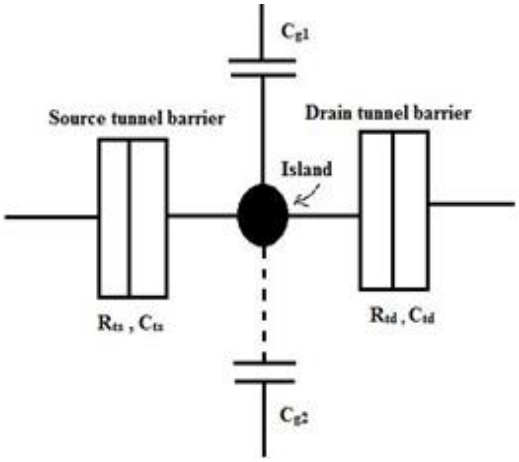

Fig. 1. SET Schematic.

The switching time is essential to operate SET as a switch. The switching time τ_T is based on the total device capacitance C_Σ and the tunneling resistance R_T.

$$\tau_T = R_T C_\Sigma \quad (4)$$

The switching time is short due to the Heisenberg principle that depends on the charging energy of the device E_C,

$$E_C \tau_T \geq h \quad (5)$$

The higher-order tunneling processes (like co-tunneling) can be stopped by higher tunneling resistance so-called von-Klitzing resistance.

$$R_T \gg \frac{2h}{Q^2} = 26K\Omega \quad (6)$$

B. SET Tunneling Mechanism

The tunnel junction in SET acts as opaque capacitors when no electron tunnel through them. Before any electron tunneling, the potential of the island is expressed as

$$V_{island} = \frac{C_g}{C_\Sigma} V_{gs} + \frac{C_{td}}{C_\Sigma} V_{ds} \quad (7)$$

The electron tunneling can take place only if $|V_{island}| > \frac{e}{2C_\Sigma}$ through the source tunnel barrier or if $|V_{ds} - V_{island}| > \frac{e}{2C_\Sigma}$ through the drain tunnel barrier. To understand the mechanism let us keep V_{ds} constant at $\frac{e}{2C_\Sigma}$ also, vary V_{gs} from zero to any higher positive value, we can observe the following mechanism represented in Fig. 2.

The perpendicular lines indicate the drain (D), island (I) and source (S) terminals and the parallel lines represent the corresponding voltages. The source (V_s) is grounded and the drain is connected to $\propto$ (V_D). The black dots denote the potential of the island before electron tunneling takes place. The white dots denote the potential of the island after electron tunneling. The solid arrows denote the electron tunneling and dotted arrows denote the changes in island potential. The numbers (1,2,3,...) denote the total current conduction sequences.

- When $V_{island} < \frac{e}{2C_\Sigma}$ the potential drop across both source and drain tunnel junction is less than $\propto = \frac{e}{2C_\Sigma}$, so the device enters the Coulomb blockade, which is highlighted in Fig. 2(a).
- If V_{gs} is increased further (higher than $\propto$) then $V_{island} > \frac{e}{2C_\Sigma}$, which allows one electron to tunnel in from source terminal to island. As a result island potential is reduced by the amount of $\frac{e}{C_\Sigma}$ consequently drain tunnel junction potential becomes higher than $\frac{e}{2C_\Sigma}$,which allows one electron to tunnel out from the island to the drain terminal that is highlighted in Fig. 2(b).
- If V_{gs} is increased further (higher than $2\propto$), once again the SET enters coulomb blockade. Initially when $V_{island} > \frac{e}{2C_\Sigma}$ one-electron tunnels in from a source to the island which reduces the island potential by $\frac{e}{C_\Sigma}$. As a result, the potential drop across both source and drain junction becomes lower than $\frac{e}{2C_\Sigma}$ and that is highlighted in Fig. 2(c).
- If V_{gs} is increased further (higher than $3\propto$), as shown in Fig. 2(d) the SET comes out of Coulomb blockade as $V_{island} > \frac{3e}{2C_\Sigma}$. When$V_{island} > \frac{e}{2C_\Sigma}$, one-electron tunnels in from a source to the island that reduces the island potential by $\frac{e}{C_\Sigma}$. Since V_{island} is still higher than $\frac{e}{2C_\Sigma}$ one more electron can tunnel in from source to island hence the island potential reduces by the amount of $\frac{e}{C_\Sigma}$. The tunneling mechanism in step b will be resumed (5-->6-->3-->4-->5-->...) and a continuous current path from source to drain is re-established.

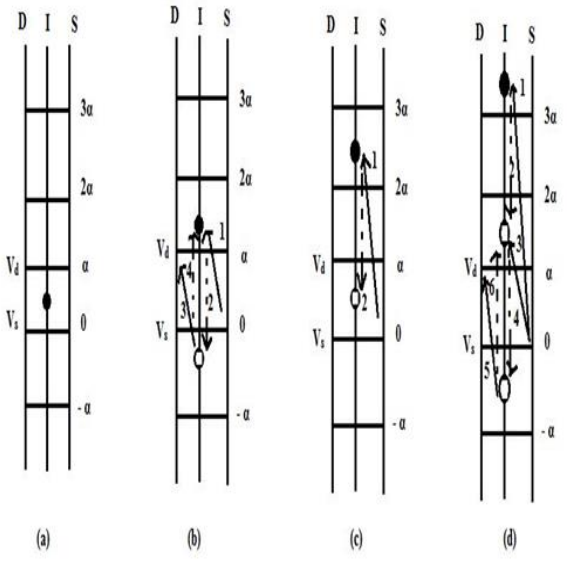

Fig. 2. Electron Tunneling Mechanism in a SET System (a-d).

III. Proposed Work

The important component of the central processing unit of a computer is an ALU, which performs arithmetic and logical operation. We proposed 4-bit SET based ALU which consists of SET based adder block, subtractor block, logical block, shifter block and a quadruple multiplexer (MUX). We designed a quadruple 4:1 MUX to select specific operation in ALU by using control signals S0 S1. We used reversible gates to perform the arithmetic operation to reduce power consumption. The proposed model of 4-bit ALU is shown in Fig. 3. Table I shows the operation table of 4-bit ALU.

We have designed the 4-bit SET based ALU which has the following features:

- Operates at a low voltage of 0.4V.
- Consumes low-power.
- Operates at high speed.
- Performs both arithmetic and logical operations.

A. SET based AND Gate

The AND gate design using single gate SET is presented in Fig. 4. The design consists of six SETs where four SETs for NAND gate design and two SETs for Inverter. Similar to static CMOS structure, the pull-up network and pull-down network are dual to each other for SET based logic gate design also. For each SET, the input is applied to gate1 and gate2 is grounded. The two gate capacitances C_{g1} and C_{g2}, drain tunnel junction capacitance C_{td} and source tunnel junction capacitance C_{ts}. We modelled symmetric SET by operating at room temperature by increasing the charging energy $E_C = \frac{e^2}{2C_\Sigma}$ which is achieved by lowering the gate capacitance and tunnel junction capacitance less than 1aF. So by increasing the temperature, the capacitance size reduces thereby feature size of island scaled-down, which narrows down the coulomb blockade region. The single gate controls the Coulomb blockade region, which regulates electron tunneling from source to drain terminal. The simulation parameters are C_{g1}=0.23aF, C_{g2}=0, C_{td}= C_{ts}=0.06aF, R_{ts}= R_{td}=1MΩ.

In a similar fashion, all logic gates have been designed using SET to design the arithmetic, logical and shifter blocks of ALU.

B. SET based Reversible Adder/Subtractor

In conventional gates, the inputs cannot be originated from the outputs, so there will be loss of one or more bit information which is dissipated as heat. Using reversible logic, the inputs can be retrieved from the outputs and vice-versa by which energy loss can be vanquished. Reversible logic gates commenced as a promising calibrating model for low power applications, quantum computing, quantum cellular automata, DNA computing and nanotechnology. To maintain the reversibility of the digital circuits, the reversible logic gate uses extra outputs known as garbage outputs.

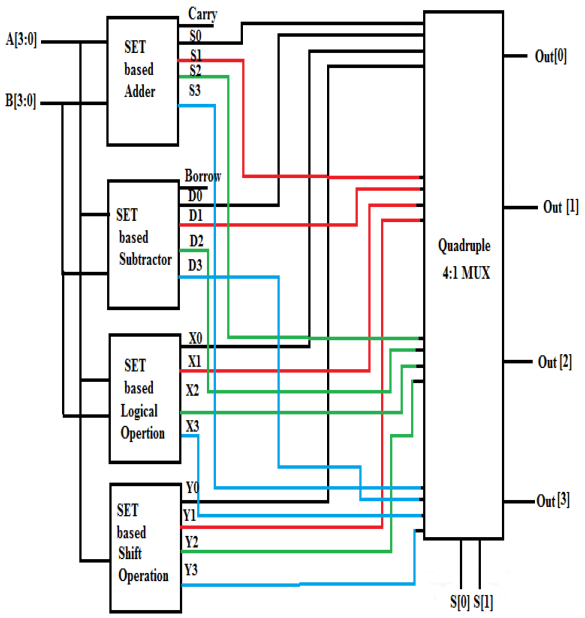

Fig. 3. SET based 4-Bit ALU Block Diagram.

TABLE. I. OPERATION TABLE OF 4-BIT ALU

S0	S1	Operation
0	0	4-bit addition
0	1	4-bit subtraction
1	0	Logical operation
1	1	Shift operation

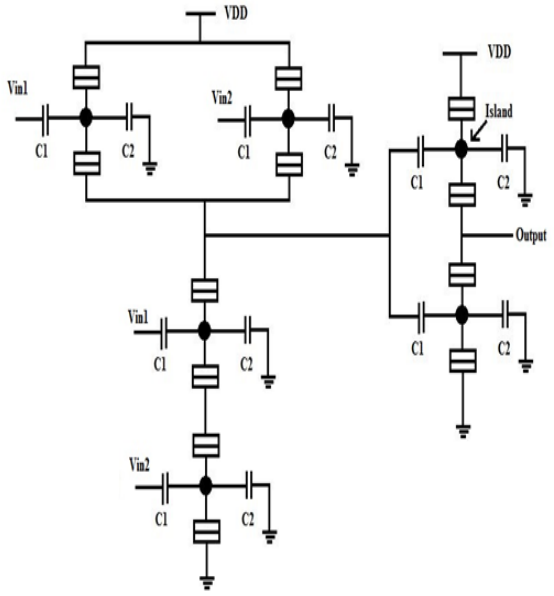

Fig. 4. SET based 2-Bit AND Gate.

In this paper, full adder and subtractor are designed using a reversible WG gate implemented using a single-electron transistor. The 4X4 WG gate design includes three inputs A, B, C and D is the control input, U, V, W and X act as outputs. By setting D=0, the circuit performs addition operation and if D=1 it performs subtraction operation. W acts as sum and X acts as carry in case of WG gate as a full adder. W acts as difference and X acts as borrow in case of WG gate as a full subtractor. The block diagram of reversible gate as full adder and subtractor are shown in Fig. 5, 6 and 7, respectively.

The circuit is simulated by using Cadence Virtuoso tool. Fig. 8 and Fig. 9 show the simulation result of SET based WG reversible full adder and full subtractor respectively. Fig. 8 shows that when the input is A=B=C=1, the circuit produces the Sum=1 Carry=1. From Fig. 9, it is analysed that when the input is A= 0 B= 1 C=1, the circuit produces the Difference= 0 Borrow=1.

C. 4-bit SET based Reversible Adder/Subtractor

We designed 4-bit reversible adder and subtractor using SET in which the SET based EXOR gate plays a significant role in determining which operation to be performed. Fig. 10 shows the block diagram of SET based reversible 4-bit adder and subtractor. When the control signal applied to the EXOR gate is set to one, it performs subtraction operation else addition operation. The circuit is simulated using 608 SETs to verify the functionality. The simulation results in Fig. 11 reveals that when the inputs A3=1 A2=0 A1=1 A0=0 and B3=0 B2=1 B1=0 B0=1 and when control is 0 the circuit performs addition operation exhibiting output as C4=1 S3=0 S2=0 S1=0 S0=0 else when control is 1 it performs subtraction operation displaying output as 10101.

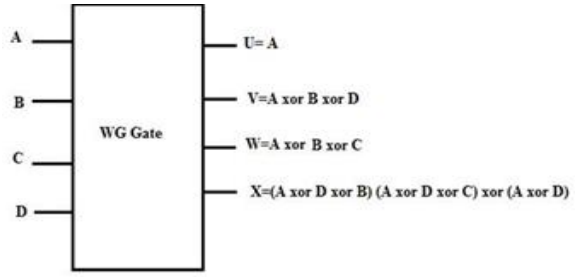

Fig. 5. WG Reversible Gate.

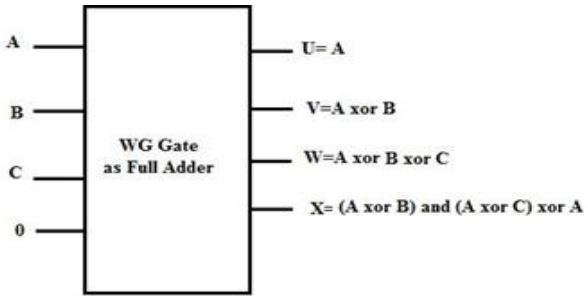

Fig. 6. WG Reversible Gate as Full Adder.

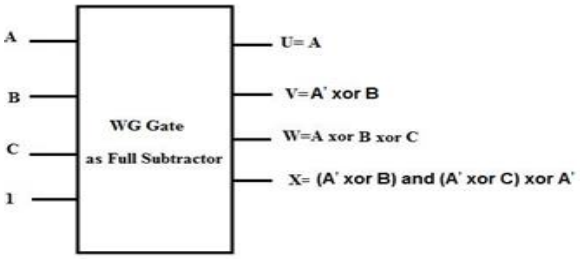

Fig. 7. WG Reversible Gate as Full Subtractor.

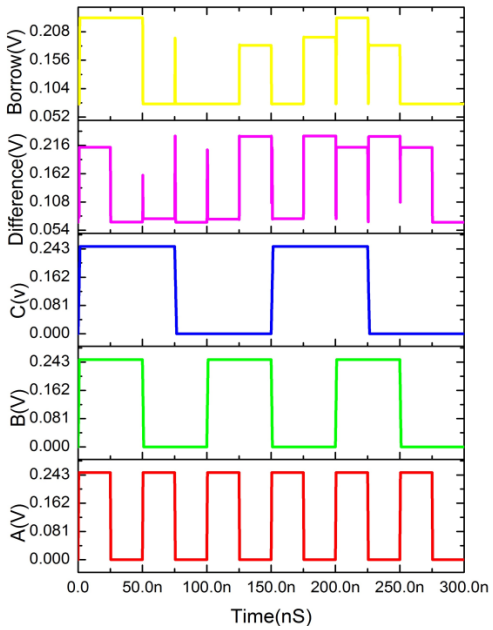

Fig. 8. Output Waveform of SET based WG Reversible Gate as Full Adder.

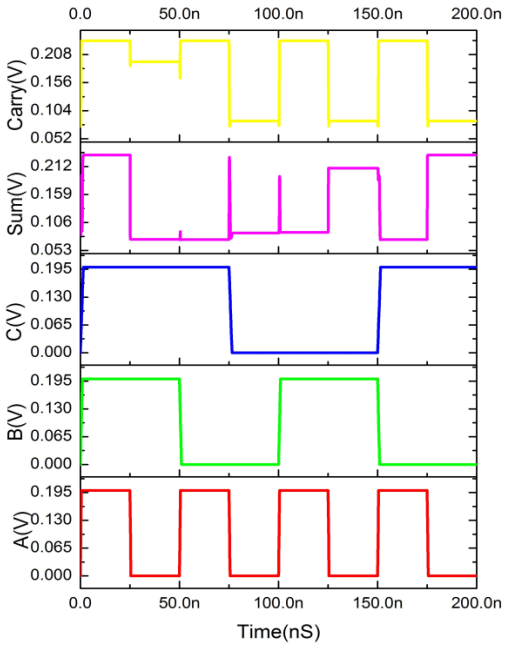

Fig. 9. Output Waveform of SET based WG Reversible Gate as Full Subtractor.

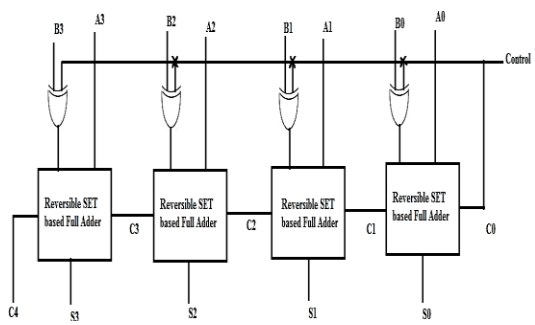

Fig. 10. 4-bit SET based Reversible Gate Full Adder/ Full Subtractor.

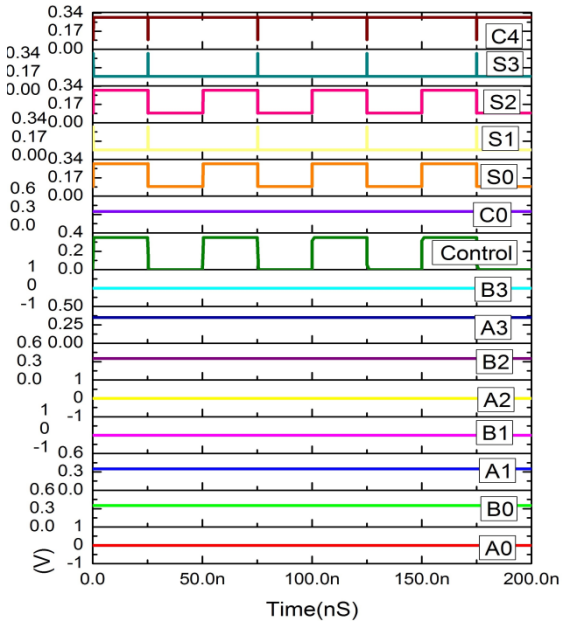

Fig. 11. Output Waveform of 4-bit SET based Reversible Gate Full Adder/ Full Subtractor.

D. 4:1 SET based Multiplexer

The 4:1 MUX is designed using SET based AND and OR gates to select the specific operation of the ALU based on the control signals S0, S1. The control signals, S0 and S1, are used to specify various actions, as given in Table II. Fig. 12 reveals the circuit is simulated using 54 SETs to verify the functionality. The block diagram of SET based 4:1 multiplexer is presented in Fig. 13.

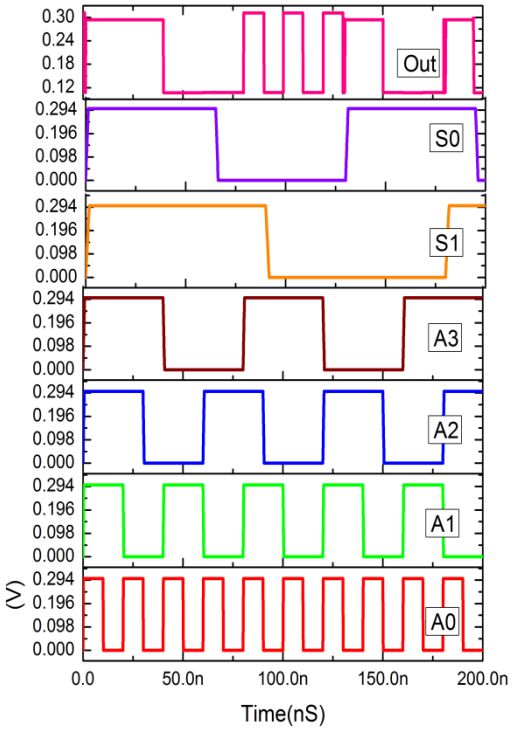

Fig. 12. Output Waveform of 4:1 SET based Multiplexer.

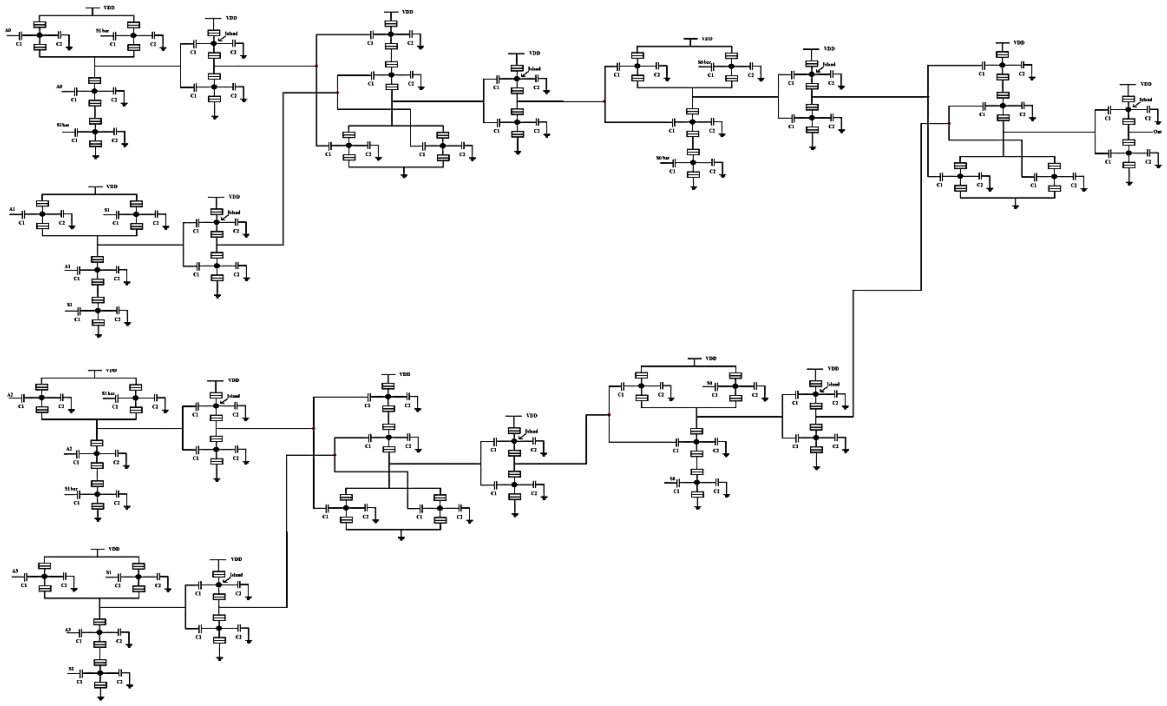

Fig. 13. 4:1 SET based Multiplexer.

TABLE. II. OPERATION TABLE OF 4:1 MULTIPLEXER

S0	S1	Out
0	0	A0
0	1	A1
1	0	A2
1	1	A3

E. 4-bit SET based Left/Right Shift Register

The shift registers are used for transfer or storage of binary data, which are generally used in computers or calculators to store binary data. A shifter is used to shift the data to the left or right side by a fixed number of positions. The vacant position is filled with zero. We designed a 4-bit logical shifter using SET based multiplexer. The selection signals, S0 and S1, are used to specify the various actions, as given in Table III. The block diagram of SET based Left/Right Shift register is shown in Fig. 14. We simulated the circuit using 204 SETs with a supply voltage of 400mV to verify the functionality. Fig. 15 shows that when the input A3=1 A2=1 A1=0 A0=1 and when the control signal S0S1=10, the input data is shifted right side providing the output as Out3 Out2 Out1 Out0 = 0110. When S0S1=11, it performs left shift operation providing the output as 1010.

F. 4-bit SET based Magnitude Comparator

A comparator compares two binary numbers of 4-bit size and generates three outputs, such as equal, greater and smaller. We have designed a magnitude comparator using SET based logic gates like INVERTER, EXNOR gate, AND gate and OR gate as shown in Fig. 16.

The condition of A>B in a 4-bit comparator can be possible in the following cases as shown in Fig. 17.

- If A3 B3 = 1 0
- If A3 B3= XX and A2 B2 = 1 0
- If A3 B3=XX, A2 B2 = XX and A1 B1 =1 0
- If A3 B3= XX, A2 B2= XX, A1 B1=XX and A0 B0 =1 0

In the same way A<B condition can be possible in the following cases:

- If A3 B3 = 0 1
- If A3 B3= XX and A2 B2 = 0 1
- If A3 B3=XX, A2 B2 = XX and A1 B1 =0 1
- If A3 B3= XX, A2 B2= XX, A1 B1=XX and A0 B0 =0 1

Where X can be either 0 or 1 treated as don't care.

The A=B condition is applicable when all the independent bits match exactly with resemblant bits of other number. We simulated the circuit using 206 SETs to verify the functionality as shown in Fig. 18.

TABLE. III. LEFT / RIGHT SHIFT OPERATION TABLE

S0	S1	Operation	Out3	Out2	Out1	Out0
0	0	No change	A3	A2	A1	A0
0	1	No change	A3	A2	A1	A0
1	0	Right shift	0	A3	A2	A1
1	1	Left shift	A2	A1	A0	0

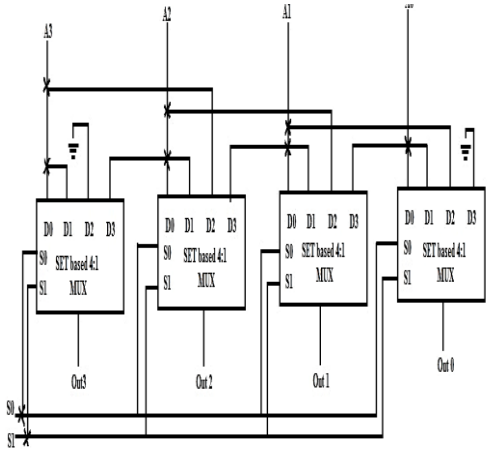

Fig. 14. 4-bit SET based Left/Right Shift Register.

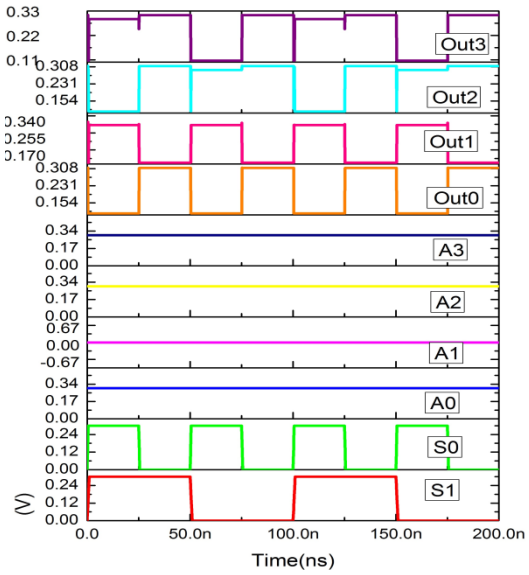

Fig. 15. Output Waveform of 4-bit SET based Left/Right Shift Register.

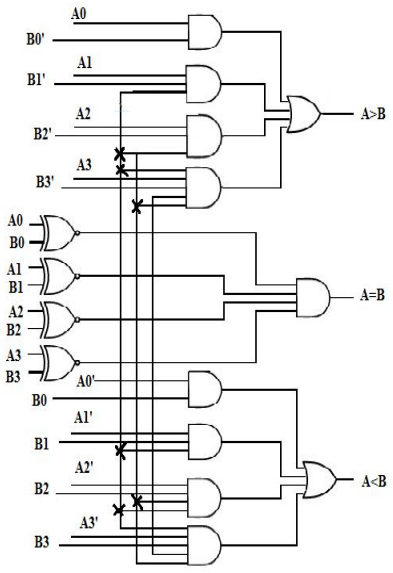

Fig. 16. 4-bit SET based Magnitude Comparator.

Comparing Inputs				Cascading Inputs			Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A < B	A = B	A > B	A < B	A = B	A > B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

Fig. 17. 4-bit Magnitude Comparator Operation Table.

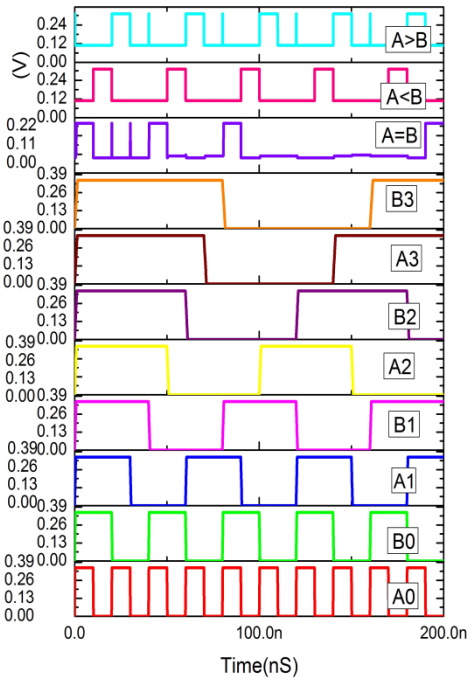

Fig. 18. Output Waveform of 4-bit SET based Magnitude Comparator.

IV. Results and Discussion

In this section, the functional simulation of SET based ALU is presented initially and later, the performance evaluation in terms of power and delay. We simulated the proposed ALU with 1554 SETs using MIB model. The control signals (S0, S1) are used to select one among various operations to determine the final output. Fig. 19 shows that when the inputs A3=1 A2=0 A1=1 A0=0 and B3=0 B2=1 B1=0 B0=1 and the control signal S0S1=00, the circuit performs addition operation providing output Carry=Out[3]= Out[2]= Out[1]= Out[0]=10000. When control signal S0S1=01, it acts as subtractor and provides output 10101. When the control signal S0S1=10, it is logical AND operation with output 0000. When control signal S0S1=11, the data is shifted left and the result is 0100. The performance evaluation of the proposed SET based ALU is shown in Table IV. The

symmetric SET based 4-bit ALU operates at room temperature with a supply voltage of 400mV exhibits power of 0.52nW and propagation delay of 350pS.

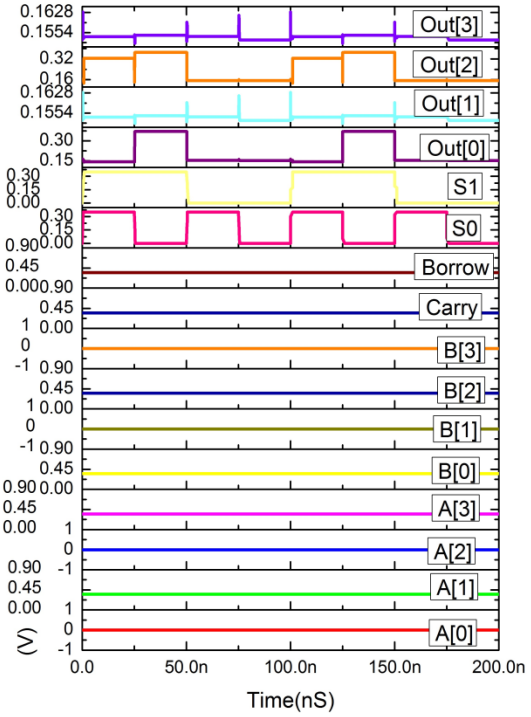

Fig. 19. Output Waveform of 4-bit SET based ALU.

TABLE. IV. PERFORMANCE ANALYSIS

Si.No	Parameters	Evaluated
1.	Number of SETs	
a.	4-Bit Adder	304
b.	4-Bit Subtractor	304
c.	4-Bit Left/Right Shifter	204
d.	4-Bit Logical Operator	24
e.	4-Bit ALU	1554
2.	Delay	350pS
3.	Power	0.52nW
4.	VDD	400mV

V. CONCLUSION

The nanodevices have unique properties such as small size and have the ability to operate at low voltage can be used for designing ultra-low-power digital circuits. Based on this property, we implemented logic circuits using the SET and developed 4-bit ALU. The proposed ALU can handle arithmetic and logical operations using two inputs of four-bit size and two control inputs to select a particular operation. The results show that the proposed ALU exhibits the power of 0.52nW and a delay of 350pS. The proposed ALU can be designed using double gate SET (DGSET) in which two gates control single electron tunneling which offers low power consumption. The proposed SET based ALUs can also be used in the implementation of quantum computers making significant improvements in the design of electronic circuits.

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