

A Novel Two Level Edge Activated Carry Save Adder for High Speed Processors

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Abstract—In today's increasing demand of higher integration levels of VLSI and ULSI processors memory capacity and ALU efficiency plays a critical role in designing. The chip-size of memory depends on number of Flip-Flop's (FF) which are the micro cells to store binary values. An efficient adder is always a parameter to estimate the cost effectiveness of multipliers used by ALU. In this paper the authors focuses on frequency clock utilization and also on low power consumption. It presents a novel Carry Save Adder (CSA) combined with the concept of two level clock triggering for high speed integrated circuits. The authors proposes a new Two Level Edge Triggered (TLET) FF's built with 14Transistors (14T) and 12Transistors (12T), efficient in terms of switching power dissipation and delay in this paper. The innovative idea deals with CSA 14T and 12T which is compared in terms of Switching Power Dissipation (SPD) from 0.8V to 2.0V. The difference in SPD from 0.8V to 2.0V supply voltage analysis is 132.0nWatts for CSA using 16T FFs, 85.6nWatts for CSA using 14T and only 70.3nWatts for CSA using 12T FFs. In this paper, there is full utilization of clock signal.

Keywords—Carry Save Adder; digital integrated circuits; flip-flop; switching power dissipation; two level edge triggering

I. INTRODUCTION

In present scenario, technology is evaluated by its computational procedures. In industry, digital implementation is prioritized by structural design for high yield adder in electronic architectural process. Field Programmable Gates Array (FPGA) consists of numerous configurable logic gates [1]. The FPGA targets the design of the architecture according to the market requirement. It aims the modular architecture arithmetic theory to increase the system performance with the utilization of clock signal. Dual Data Rate in Very Large Scale Integration circuits has come into existence and many circuits were proposed in Two Level Edge Triggered FFs [2-5]. In order to increase Clock performance two edges of the Clock are used to trigger the FFs, this increases the clock frequency. A pulse activated memory cell (FF) is inbuilt with pulse generator and a bi-stable latch for putting away parallel qualities. The circuit intricacy and number of stages inside these pulse activated FF are decreased for D to Q delay reduction. Clock edge activated FF's are extensively two kinds Implicit Pulse activated FF and Explicit Pulse activated FF [6]. In implicit pulse activated FF the clock is created inside the FF, for occurrence, information near yield, Hybrid Latch FF (HLFF) and Semi switching FF (SFF) [6].

In Explicit pulse initiated FF (E p-FF), the pulse is delivered remotely with the aim, that all the neighboring FFs can share the clock. Frameworks like Explicit Pulse Triggered Data Close to Output (EP DCO), static Conditional Discharge FF (S-CDFF) [7] is the crucial arrangement techniques of Ep-FF. Pulse-based FF is mainly for its soft-clock edge property, which allows time borrowing and reduces clock skew[8]. It also deploys superior latency incorporating complex logic. Some of the recently proposed Two Level Edge Triggered FF's are EXDCO [8]

It uses NAND-logic gates for clock generation; the power consumption of Clock Generator is less because transistor ON time for MN2 is less. But Data input(D) to Data out (Q) path of the FF shows more delay as D has to traverse through transistors MN1 and MN2 and clock has to switch MN3 transistor. Node X in the circuit shows more discharge time which results in positive Set-up time. In order to avoid discharge at node X in EP-DCO DETFF a new idea called Explicit Pulse Triggered Conditional Discharge FF (EXCDFF) is proposed in [8].

16T Improved Two Level Edge Triggered FF (ITETFF) is obtained just by substituting transmission gates of Clock input with n-MOS switches [9]. It has two data paths from Data in (D) to Data out (Q) shows master slave FF features. As n-MOS transistor along with CMOS inverter is used to latch it stores both strong-'0' and strong-'1'. The 16T ITFETFF is free from edge voltage loss issues of pass transistor. By utilizing NMOS transistor in transmission gates .By supplanting the p-type pass transistor by n-type transistor we can diminish the area due to NMOS is smaller than PMOS transistor. It is remunerated that portability requirement of NMOS and PMOS. In this way recently altered two level edge activated FF is progressively proficient in region, power and speed when contrasted with past FF.

The concept of two levels Edge triggering is combined with CSA to enhance the performance of adders thereby improving the speed of multipliers.

The selection of suitable adder with obligatory properties is characterized by different features [10-13]. In this paper the case study the more important criteria which is highlighted is low power and high frequency which is considered these days for internet of things applications. The Adders plays a major role in Signal processing, Image processing and VLSI Applications [14-19]. Demand for elevated speed and low power adders have led to focus on the design strategies of

resourceful adders. They not only work as arithmetic logic unit in computers and some processors but they are used to determine addresses, table directories, and parallel operations Binary adders with enormous variety of algorithms and executions [20].

In CSA parallel architectural execution expands the benefit to provide significant progress [19-22]. The computational performance executes with quite an assortment of operands.

The n-bit adder of two numbers:

$$X = x_{i-1}, x_{i-2} \dots x_0 \text{ and}$$

$$Y = y_{i-1}, y_{i-2} \dots y_0$$

Resulting in the n-bit sum,

$$S = s_{i-1}, s_{i-2} \dots s_0 \text{ and an output carry, } C_{out}.$$

The primary phase in CSA computes the bit generate and bit propagate as follows:

$$G_i = x_i \cdot y_i \text{ and}$$

$$P_i = x_i + y_i \quad \dots \quad (1)$$

Where G_i is the bits generate and P_i is the bits propagate. These are then utilized to compute the final sum and output carry bits, with the help of equations (2):

$$S_i = P_i \oplus C_i \text{ an}$$

$$C_{i+1} = G_i + P_i \cdot C_i \quad \dots \quad (2)$$

In contemporary semiconductor industry total power dissipation in CMOS IC's due to leakage current and the leakage power. The static and dynamic power dissipates exponentially which effects efficiency and value of the system [23]. The most highlighted basis for consuming switching power dynamically is the gate capacitance, load capacitance and wiring capacitance. The mathematical relation is expressed in equation (3).

$$P_{switch} = \frac{1}{2} C_{Total} V_{DD}^2 \quad \dots \quad (3)$$

$$C_{Total} = C_{Gate} + C_{load} + C_{interconnect} \quad \dots \quad (4)$$

C_{Gate} = Total gate capacitance

C_{load} = variable Load Capacitance

$C_{interconnect}$ = Total interconnect capacitance

Leakage power in CMOS circuits is contributed by leakage currents in each transistor given by the equation (5).

$$I_{leak} = I_{SUB} + I_{RB} + I_G + I_{GIDL} \quad \dots \quad (5)$$

I_{SUB} = subthreshold leakage current

I_{RB} = Reverse bias leakage current

I_G = Gate Tunneling Current

I_{GIDL} = Gate Induce Drain Leakage Current

Subthreshold leakage current (I_{SUB}) and gate tunneling leakage current (I_G) are identified as key sources of leakage currents in all transistor. Subthreshold leakage current transpires only in turned-off transistors [24], [25]. For an individual device, leakage current can be calculated by equation (6).

$$I_{sub} = K_1 W e^{-\frac{V_{threshold}}{\sigma v T}} \left(1 - e^{-\frac{v_{dd}}{v T}} \right) \quad \dots \quad (6)$$

Where

$$v T = \frac{k T}{q} \dots \quad (7)$$

In this paper leakage current variation of CSA using 16T, 14T and 12T is done by varying temperature from -40C to 120C. Fast Fourier Transform FFTs are comprehensively applied in Image Processing, data compressions, Signal spectral analysis, filtering signals, etc. In Biomedical field, Medical Imaging plays an important role for various health conditions. Electrocardiography (ECG) and Electroencephalography (EEG) are an assortment of techniques to learn the pattern of signals generated by heart and brain. Addition and multiplication operations are two fundamental analysis blocks to carry out FFT. As higher order adders contribute to larger amounts of delay and energy consumption slowing down the performance of FFT [26]. This implies the proposed adder can be efficiently used for high speed processors.

The DFT is analysis of a discrete-time sequence $f(m)$ in frequency domain representation. The M-point DFT of finite-duration sequence $f(m)$ is defined as $F(k)$.

$$F(k) = \sum_{m=0}^{M-1} F(m) \cdot \sum_{m=0}^{kM} W \quad \dots \quad (8)$$

Where W refers to twiddle factor defines as

$$W = e^{-j2\pi m/M} \quad \dots \quad (9)$$

The progress of high-speed algorithms, known as FFTs, has made execution of DFT levelheaded in real-time applications. The Fast Fourier Transform (FFT) and the Energy Scattered spectrum (ESS) are dominant tools for scrutinizing and evaluating signals. The energy scattered analysis in a ESS of FFT at fundamental frequency is given by the equations (10) to (11).

$$E_{Scattered} = K [\sin\theta - P] \quad \dots \quad (10)$$

Where K is spring constant, Q is the Q-factor of ESS and θ is phase of fundamental frequency.

$$K = (\pi k P_0 P_1) / Q \quad \dots \quad (11)$$

and P is Perturb ratio, P_1 and P_0 are Perturbed amplitudes.

$$P = P_1 / P_0 \quad \dots \quad (12)$$

FFT investigation of CSA using 16T, 14T and 12T TLETF is done with the help of ESS. CSA using 12T displays less energy consumption at fundamental frequency Fig. 1.

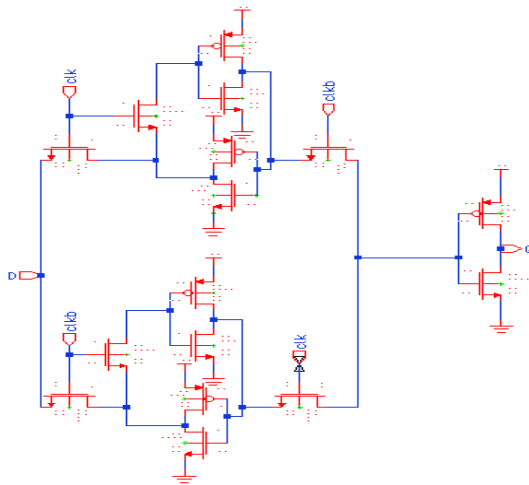


Fig 1. 16T-TLETFF Memory Cell Circuit Diagram.

II. PROPOSED TECHNIQUES

A. 14T Improved Two Level Edge Triggered FF (TLETFF-1)

A different TLETFF1 is proposed by modifying the 16T FF, the two n-mos transistors connecting back to back inverters are removed. From the circuit in Fig. 2, we observe that, in the upper Din to Q path n-mos transistors switching for clk used for the same read operation during positive edge, and bottom path clk signal switches n-mos connecting inverters for read operation. In a single data path two transistors switch for the same edges of the clock for same operation n-MOS transistors connecting back to back inverters are removed. This reduces the transistor count to 14 and the working of new 14T TLETFF is shown in Fig. 2.

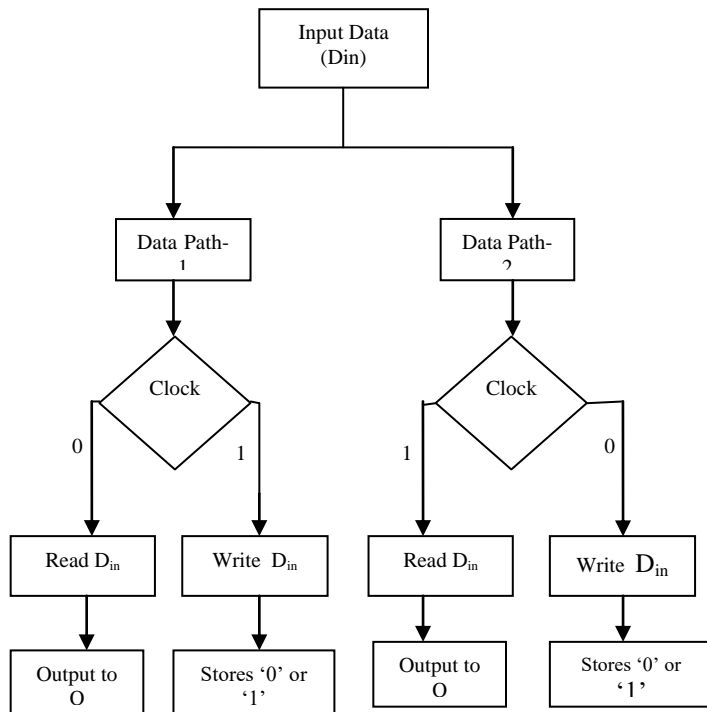


Fig 2. Circuit Diagram of Novel 14T TLETFF-2.

B. Improved Two Level Edge Triggered FF-2 (TLETFF-2)

In Improved Two Level Edge Triggered FF the upper data path-1 is activated on '0' to '1' rising edge and lower datapath-2 is activated on '1' to '0' falling edge. In this memory cell an inverter and a PMOS transistor shapes a bi-stable component to hold the bit value. This reduces the transistor count to 14. The working of new 12T TLETFF is shown in Fig. 3.

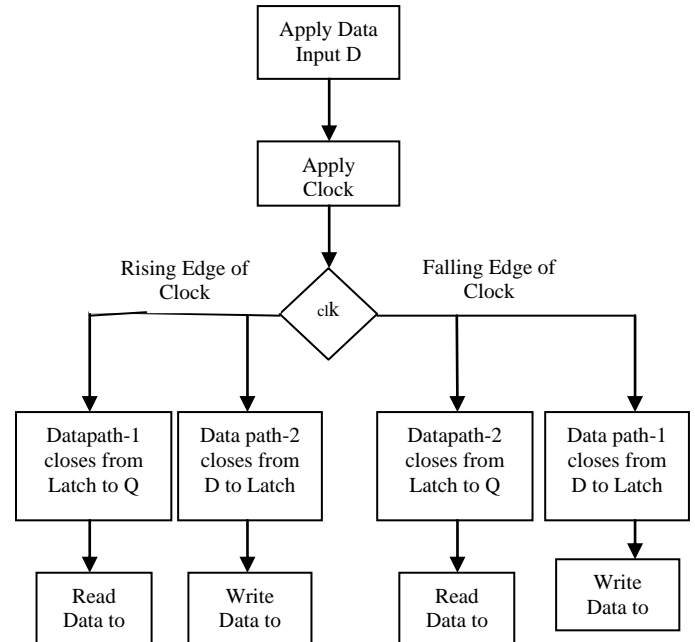


Fig 3. Circuit Diagram of Novel 12T TLETFF-1.

III. CARRY SAVE ADDER (CSA) USING TWO LEVEL EDGE TRIGGERED FFs

As Dual Data Rate VLSI circuits have appeared numerous circuits were proposed in Two Level Edge Triggered FFs. So as to expand Clock execution two edges of the Clock are utilized to trigger the FFs, this builds the clock recurrence. Beat based FF is for the most part for its delicate clock edge property, which permits time getting and diminishes clock slant. It additionally gives predominant inertness and is equipped for joining complex rationale [13-15]. CSA's are the fastest and accurate adders used in high speed processor applications. The frequency of generating the sum bits can be doubled by applying the concept of TETFF's. The intermediate carry bits are stored in flip flops until individual sum bits are generated and summed up to get the final sum and carry out. In Fig. 5, CSA using 14T TLETFF A and B are 6-bit wide inputs where A="010101" B="000100" and Carry Input Cin='0' the logic circuit output sum is from S5 to S0 which is equal to "110010" and Cout='0'.

AND gate output is the intermediate carryout stored in 14T TLETFF and given as the input to Ex-or gate. The second input to EX-OR gate present at output is the next corresponding bits sum. By introducing TLETFF to save the carry bits the frequency of operation is doubled and clock efficiency increases to 100%. In CSA using 12T TLETFF A and B are 6-bit wide inputs where A=B="100011" and Carry Input Cin='1' the logic circuit output sum is from S0 to S5

which is equal to “000111” and Cout= ‘1’. For the CSA implemented using 12T and 14T the clock frequency is equal to the frequency at which sum bits are generated. By The results of CSA using 14T and 12T are compared in terms of power, delay and leakage currents for 6-bit and extended up to 32-bit CSA adder.

IV. RESULTS AND DISCUSSIONS

A. Power and Delay Analysis of Two Level Edge Triggered FFs:

All the circuits are functionally verified and calculations using Mentor Graphics is done at 45nm technology. Area (number of transistors), Delay and Power comparisons of Carry Save Adder using 16T, 14T and 12T Two level Edge Triggered FFs are evaluated. Carry Save Adder using 12T shows efficient results when compared to previous methods. The outputs sum and carryout of adder can be seen at all edges of the clock signal.

Fig. 4 shows the switching power dissipation of 16T, 14T and 12T FFs. The delta change between maximum (at 100fF) and minimum (0fF) power dissipation of 16T FF is 51μW, for 14T it is 44 μW and for 12T it is 37μW. switching power of 12TFF is reduced by 27.4% when compared to 16T FF. 14T FF’s switching power is reduced by 13.5% when compared with 16T FF. 12T FF shows more percentage reduction in power when compared with 14T.

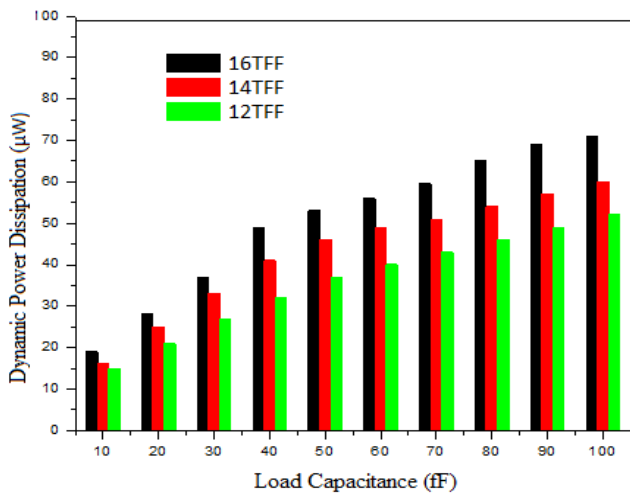


Fig 4. Switching Power Dissipation versus Load Capacitance.

B. Delay Analysis

There are 4 timing parameters Rise transition time, Fall Transition time, Propagation delay high-low and propagation delay low-high Rise Transition time (t_r) is the delay, during progress, when yield changes from 10% to 90% of the most extreme worth. Fall transition time (t_f) is the delay, during progress, when yield changes from 90% to 10% of the greatest worth. Numerous structures could likewise lean toward 30% to 70% for rise time and 70% to 30% for fall time. It could shift up to various structures.

The proliferation defer high to low (tpHL) is the postponement when yield changes from high-to-low, after information changes from low-to-high. The postponement is

normally determined at half purpose of information yield exchanging. Table I displays the values of rise transition time and fall transition time delays calculated at variable capacitive loads from 10fF to 100fF. The slope of the delay is less in 14T FF when compared to 12T FF as the delta change of rise delay and fall delay is less. For 12T FF the rise and fall in the signal starts at 0ns where as in 14T it starts with positive value which increases the propagation delay of the FF.

Leakage current for 16T, 14T and 12T are calculated at different temperatures ranging from -400C to 1200C. 14T FF shows less leakage currents when compared to 12T FF, this is because in 12T FF a p-MOS transistor is connected in feedback loop that results in a short circuit path from Vdd of p-MOS transistor to the ground through n-MOS transistor of CMOS inverter.

From the above graphs of Fig. 4 and Table I, it is clear that 12T TETFF is efficient in terms of switching power dissipation and delay. The Leakage current increases with temperature for 12T because of p-MOS in feedback path as shown in Fig. 5.

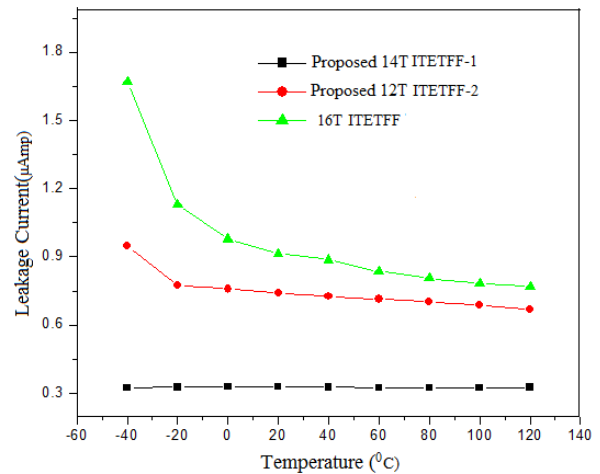


Fig 5. Leakage Current v/s Temperature.

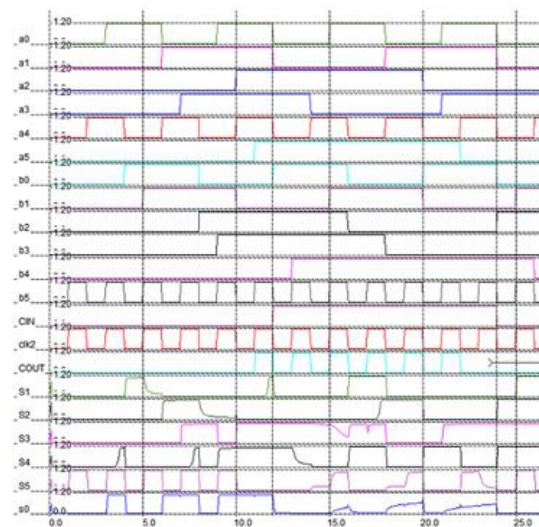


Fig 6. Output Waveform of CSA using 16T Two Level Edge Activated Flip Flop.

TABLE I. RISE TRANSITION AND FALL TRANSITION CALCULATION AT VARIOUS LOADS AT OUTPUT OF FF

Capacitance (fF)	16T TLETFF		Proposed 14T TLETFF-1		Proposed 12T TLETFF-2	
	Tr(nsec)	Tf(nsec)	Tr(nsec)	Tf(nsec)	Tr(nsec)	Tf(nsec)
10	0-0.328	0.03-0.331	0.043-0.216	0.023-0.064	0-0.214	0-0.214
20	0-0.398	0.03-0.397	0.062-0.340	0.062-0.340	0-0.339	0-0.339
30	0-0.419	0.03-0.423	0.080-0.454	0.080-0.454	0-0.454	0-0.454
40	0-0.589	0.03-0.597	0.093-0.563	0.093-0.563	0-0.564	0-0.564
50	0-0.735	0.03-0.764	0.085-0.668	0.085-0.668	0-0.670	0-0.670
60	0-0.810	0.03-0.830	0.068-0.770	0.068-0.770	0-0.773	0-0.773
70	0-0.938	0.03-0.989	0.051-0.870	0.051-0.870	0-0.873	0-0.873
80	0-1.190	0.03-1.210	0.032-0.968	0.032-0.968	0-0.972	0-0.972
90	0-1.370	0.03-1.440	0.024-1.160	0.026-1.260	0-1.068	0-1.068
100	0-1.570	0.03-1.690	0.16-1.210	0.091-1.240	0-1.120	0-1.120

4.3 Performance analysis of CSA using Two Level Triggering

The following paper discusses on implementation and evaluation of Carry Save Adder using three types of flip flops. Fig. 7, 8 and 9 shows the output waveforms of 6-bit CSA using 16T FF, 14T FF and 12TFF. The carry output is generated at two edges of clock, this is because of the two level edge triggered flip-flop incorporated into adder.

The above waveform in Fig. 6 shows sum and carry output of CSA using 16T flip flop. Sum bits from S0 to S5 are highly distorted due to glitches. The delay of carry output with respect to carry in is 904.7 ps at a clock frequency of 1GHz, which is high when compare to CSA using 14T and 12T FF.

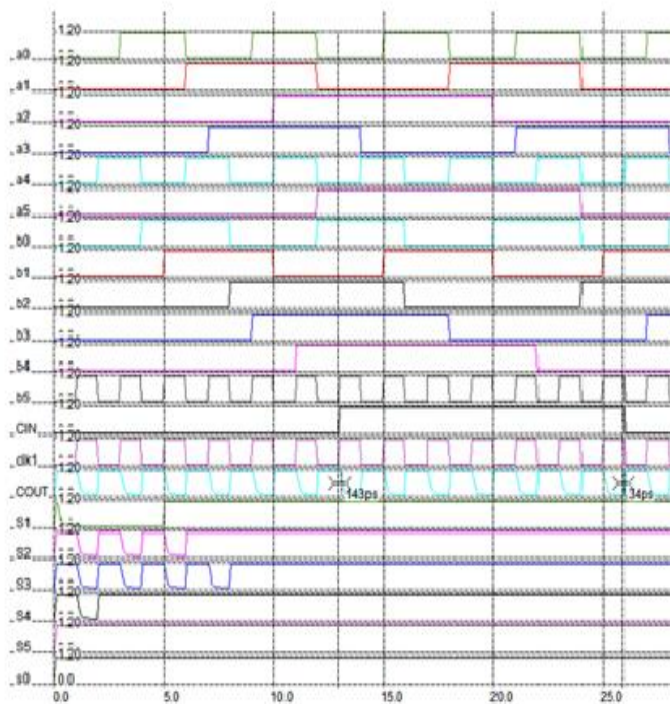


Fig 7. Output Wave Forms of CSA using 14T Two Level Edge Triggering.

Fig. 7 and 8 shows the sum and carry output waveforms of proposed two techniques. The sum outputs from S0 to S5 are free from glitches and are smooth. From the two waveforms it can be observed clearly that carry output is generated at all the edges of the clock signal.

Fig. 9 shows the distribution of transition delay of carry output with respect to carry input at different output loads. Capacitances differing from 0fF to 100fF is connected to the carry output of the CSA circuit designed using 16T, 14T and 12T TLETFF. The delay in CSA using 12T TLETFF is reduced by 27% when compared with 16T TLETFF. The maximum transition delay of CSA implemented using 12T TLETFF is only 1.109nsec. The percentage reduction in delay for 14T TLETFF with respect to CSA using 16T TLETFF is 16.2%. Table II shows switching power dissipation of CSA using existing and proposed two level edge triggered flip flops. The variation in power dissipation from 0.8v to 1.2 volts is 133.5nWatts for CSA using 16T TLETFF, 86.1nWatts for CSA using 14T TLETFF and 70.5nwatts for CSA using 12T TLETFF. It can be inferred that CSA using 12T FF shows more desirable result when compared to previous techniques. This shows 12T flip flop can be used for a wide range of fluctuating voltages.

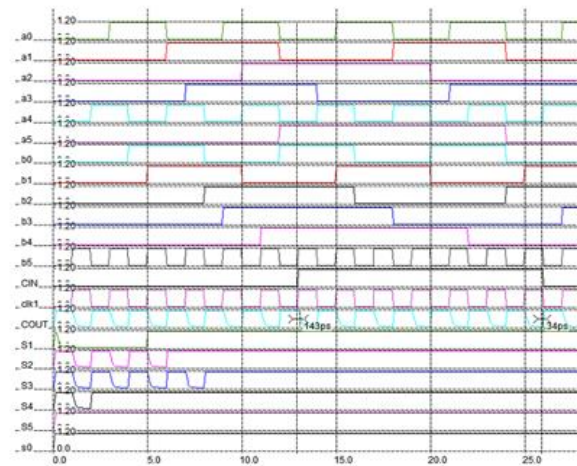


Fig 8. Output Wave Forms of CSA using 12T Two Level Edge Triggering.

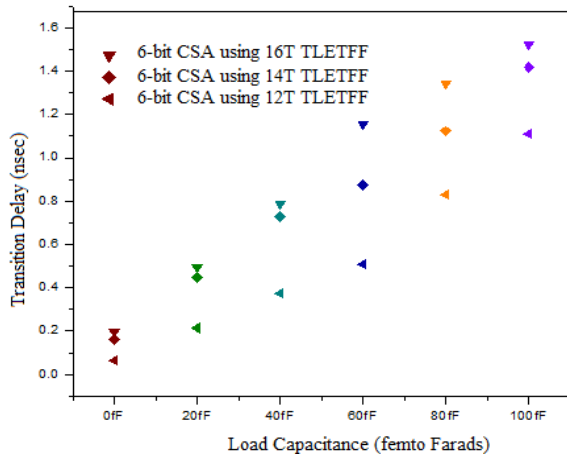


Fig 9. Delay Comparison of Carry out w.r.t Carry in.

TABLE II. SWITCHING POWER DISSIPATION OF CSA USING TWO LEVEL EDGE TRIGGERING.

Supply Voltage (Volts)	Switching Power Dissipation (nWatts)		
	CSA Using 16T TLETFF	CSA Using 14T TLETFF	CSA Using 12T TLETFF
0.8	65.2	55.4	36.0
1.0	66.4	58.0	42.1
1.2	72.1	59.3	49.2
1.4	74.0	72.0	66.5
1.6	77.4	77.6	75.8
1.8	89.0	97.6	82.1
2.0	198.7	141.5	106.5

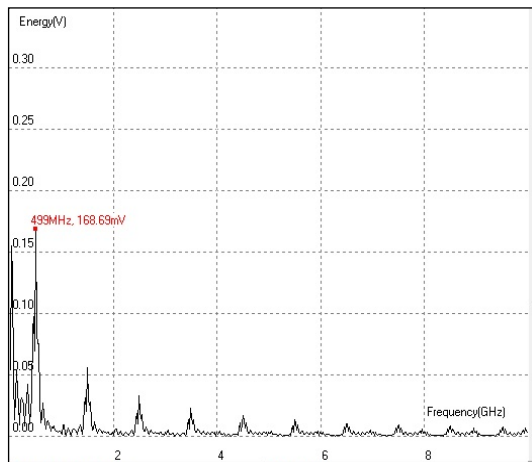


Fig 10. ESS at Fundamental Frequency of CSA using 12T FF.

Using low power, area efficient as well as high speed multipliers and adders in Fast Fourier Transform (FFT) will guarantee upgraded execution and effectiveness. The graphs shown below are the FFT analysis of CSA constructed using 12T, 14T and 16T TLET FFs. The Energy dissipation at fundamental frequency for 12T is less when compared to 14T and 16T TLETFF's. Fig. 10, 11 and 12 shows FFT analysis done from a frequency range of 250 MHz to 8GHz. It is clear that Energy dissipated at fundamental and resonant frequencies is less for 12T. Throughout the above discussion we conclude that adder using 12T can be used for high speed DSP processors.

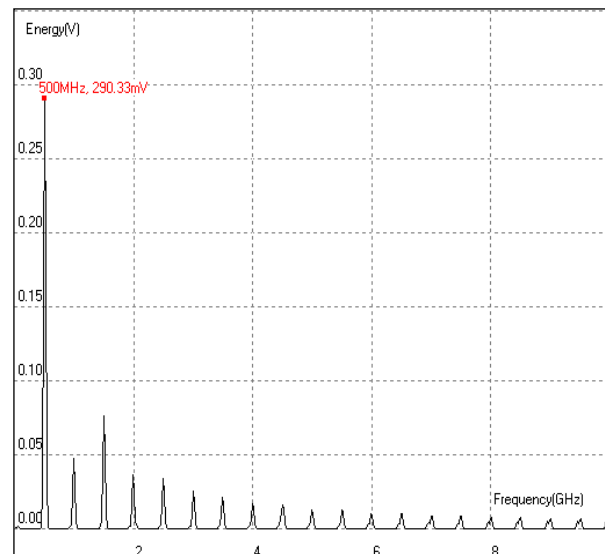


Fig 11. ESS at Fundamental Frequency of CSA using 14T FF.

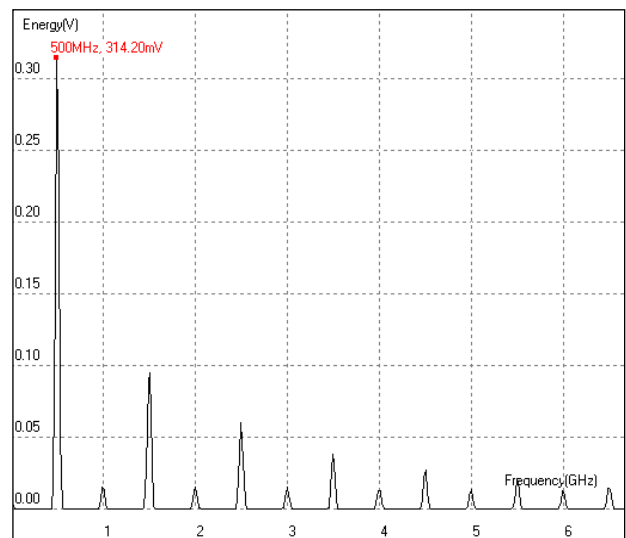


Fig 12. ESS at Fundamental Frequency of CSA using 16T FF.

V. CONCLUSION

The ESS graphs clearly shows energy dissipated for CSA using 12T TLETFF is only 168.9mV where as for 14T it is 290.33mV and for 16T it is 314.20mV at fundamental frequency. 12T TLETFF shows better performance in terms of power and delay with reduced area. Due to p-MOS transistor connected in bi-stable element of 12T FF leakage current is more when compared to both 14T and 16T FFs. Carry Select adder implemented using Two Level Edge Triggering generates the carry output both at rising edge and the falling edge of the clock which improves clock efficiency to 100%. Variation in transition delay from no-load to 100fF of carry output of CSA using 12T is less when compared with CSA using 14T and 16T TLETFF. The percentage reduction of switching power dissipation of CSA using 12T at 1.2 volts is reduced by 46.42% with that of existing technique and for CSA using 14T it is reduced by 28.78%.

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