Optimized Design of a Converter Decimal to BCD Encoder and a Reversible 4-bit Controlled Up/Down Synchronous Counter

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***Abstract*—The field of quantum computing, reversible logic, and nanotechnology have earned much attention from researchers in recent years due to their low power dissipation. Quantum computing has been a guiding light for nanotechnology, optical computing of information, low power CMOS design, computer science. Moreover, the dissipation of energy in the field combinatorial logic circuits becomes one of the most important aspects to be avoided. This problem is remedied by a reversible logic favoring the reproduction of inputs to outputs, which is due to the absence of unused bits. Every bit of information not used generates a loss of information causing a loss of energy under the form of heat, the reversible logic leads to zero heat dissipation. Among the components affected by reversible logic are binary reversible counter and converter from decimal to BCD encoder(D2BE) which are considered essential elements. This article will propose an optimized reversible design of a converter from decimal to BCD encoder (D2BE) and an optimized design of reversible Binary counter with up/ down. Our designs show an improvement compared to previous works by replacing some reversible gates with others while keeping the same functionality and improving performance criteria in terms of the number of gates, garbage outputs, constant inputs, quantum cost, delay, and Hardware complexity.**

Keywords*—Decimal to BCD Encoder (D2BE); Reversible Binary Counter; Number of Gates (CG); Number of Garbage Output (NGO); Number of Constant Inputs (NCI); Quantum Cost (QC); Hardware Complexity (HC)

I. Introduction

In the irreversible logic, the design of circuits becomes more and more difficult in terms of material design, this is due to the dissipation of energy in the form of heat which is generated at the end of the lost or unused bits. In irreversible logical calculation, each unused bit generates a loss of energy which is expressed by the formula KTln2 or K: constant of BOLTZMAN and T: absolute temperature related to calculation, this formula was established by Landauer in 1960 [1]. In digital circuits, energy loss is a function of garbage outputs (unused bits). Bennett has proven that this loss of energy can be avoided by a reversible logic using reversible gates [2]. Toffoli [3] shown in 1980 that to avoid a zero internal power circuit, it can be designed using reversible logic gates which, inside each of them, have a certain bijectivity [4-6] between inputs and outputs. Each reversible gate must have a tie between the number of inputs and that of outputs [4-6] and each input vector can be uniquely deduced from the output vector [4-6]. Performance criteria to be improved and concerned by this study are: Number of gates (CG), Number of garbage outputs (NGO) The number of constant inputs (NCI) and Quantum cost (QC). Fredkin and Toffoli have shown that the more NCI and NGO are minimized, the more efficient the circuit design is improved [7]. It was shown in [8-10] that the decrease in energy dissipation in the form of heat is proportional to the minimization of the NGO which shows the great importance of these criteria.

Our work will be divided into two parts the first concerns the design of a converter from decimal to BCD encoder based on a recent study design6 [14]: to modify it and improve the performance criteria compared to the latter and even to the five other studies design5 [14], design4 [13], design3 [12], design2 [12] and design1 [11]. The second concerns the design of a reversible binary counter based on a recent study design3 [17]by modifying it while keeping its same functionality and increasing the performance criteria compared to the latter and even to the two other studies design2 [16] and design1 [15].

The rest of this article is organized as follows: the second section presents the reversible gates concerned by this article by showing their performance criteria, namely the quantum cost that is deducted from the associated quantum implementation, and the hardware complexity. The third section presents a literature review of the recent designs proposed related to each study the design of the converter from decimal to BCD encoder and the reversible binary counter while showing the performance criteria of each, for the first study we have six proposals designs and for the second one we have three.

The fourth section shows our proposed designs of the D2BE circuit and reversible binary counter. The fifth section will show the result and discussion of our work by revealing our proposed designs and calculate our performance criteria while showing the percentages of improvement obtained.

Finally, a conclusion and perspectives in the last section.

II. The Reversible Gates Concerned by the Study and their Performance Criteria

In this section we will define the six performance criteria concerned by this article which are:

A. Performance Criteria

1) Number of Gates (CG): The number of gates required to make a circuit [18].

2) Number of garbage outputs (NGO): The unused or unwanted logic outputs of the reversible gate maintain in the output lines to make the circuit reversible [22].

3) Number of Constant Inputs (NCI): The number of inputs must remain constant at 0 or 1 to integrate the given logic function [6].

4) Quantum Cost (QC): The QC is calculated by counting the number of one input–output and two input–output reversible gates used in realizing a circuit [19,20]. The QC of one input–output and two input–output reversible gates is realized to be 1.

5) Hardware Complexity (HC): The number of fundamental operations (Ex-OR, AND, NO, etc.) required to make the circuit. Actually, a constant complexity is supposed for each fundamental operation of the circuit, such as α for Ex-OR, β for AND, δ for NOT, etc. Eventually, the entire number of operations is calculated in terms of α, β, and δ [23].

In this part, we will present the reversible gates that we will use in this article by showing their performance criteria, specially the quantum cost that we deduce directly from the quantum implementation, and its hardware complexity.

B. Feyman Gate FG

A reversible gate 2 * 2 have as inputs A and B and as outputs P = A and Q = A $\bigoplus$ B. The quantum cost of the gate FG is worth QC = 1, its Hardware complexity is worth HC = 1α [18].

C. TS-3 Gate

A reversible gate 3 * 3 have for inputs A, B and C and as outputs P = A, Q = B and R = A $\bigoplus$ B . The quantum cost of the TS-3 gate is equal to QC = 2, its Hardware complexity is worth HC = 2 α [24].

D. Fredkin Gate FRG

A reversible gate 3 * 3 have as inputs A, B and C and as outputs P = A, Q = A'B $\bigoplus$ AC and R = A'C $\bigoplus$ AB. The quantum cost of the FRG gate is equal to QC = 2, its Hardware complexity is equal to HC = 2 α + 4 β + 1 δ [18].

E. Peres Gate PG

A reversible gate 3 * 3 have as inputs A, B and C and as outputs P = A, Q = A $\bigoplus$ and R = AB $\bigoplus$ C. The quantum cost of the gate PG is equal to QC = 4, its Hardware complexity is worth HC = 2 α + 1 β [25].

F. HNFG Gate

A reversible gate 4 * 4 have for inputs A, B, C and D as outputs P = A, Q = A $\bigoplus$ C, R = B and S = B $\bigoplus$ D. The quantum cost of the HNFG gate is equal to QC = 4, its Hardware complexity is worth HC = 2 α [18].

G. HNG Gate

A reversible gate 4 * 4 have as inputs A, B, C and D as outputs P = A, Q = B, R = A $\bigoplus$ B $\bigoplus$ C and S = (A $\bigoplus$ B) C $\bigoplus$ AB $\bigoplus$ D. The quantum cost of the HNG gate is equal to QC = 6, its Hardware complexity is worth HC = 4 α + 2 β[18].

H. RSJ Gate

A reversible gate 4 * 4 have as inputs A, B, C and D as outputs P = A, Q = B, R = AB $\bigoplus$ C, S = AB $\bigoplus$ D.The quantum cost of the RSJ gate is equal to QC = 12 and its Hardware complexity is equal to HC = 2 α + 1 β [26].

I. TFG Gate

A reversible gate 4 * 4 have as inputs A, B, C and D as outputs P = A, Q = A $\bigoplus$ B, R = AB $\bigoplus$ C, S = AB $\bigoplus$ C $bigoplus$ D. The quantum cost of the TFG gate is equal to QC = 5 and its Hardware complexity is equal to HC = 3 α + 1 β [15].

J. TKS Gate

A reversible gate 4 * 4 have as inputs A, B, and C as outputs P = AC '+ BC, Q = A $\bigoplus$ B $\bigoplus$ C, R = AC + BC'. The quantum cost and the Hardware complexity of the TKS gate is not mentioned [27].

K. MSH Gate

A reversible gate 4 * 4 have as inputs A, B, C and D as outputs P = A, Q = B $\bigoplus$ C, R = A'C $\bigoplus$ AB and S = A'C $\bigoplus$ AB $\bigoplus$ D. The quantum cost of the MSH gate is equal to QC = 6 and its Hardware complexity is equal to HC = 3 α + 2 β + 1 δ [28].

L. NP Gate

A reversible gate 4 * 4 have as inputs A, B, C and D as outputs P = A, Q = A'B $\bigoplus$ AC ', R = A'C $\bigoplus$ AB and S = A'C $\bigoplus$ AB $\bigoplus$ D. The quantum cost of the gate NP is equal to QC = 5 and its Hardware complexity is equal to HC = 3 α + 4 β + 2 δ [29].

M. BJN Gate

A reversible gate 3 * 3 have as inputs A, B and D as outputs P = A, Q = B, R = (A + B) $\bigoplus$ C. The quantum cost of the gate BJN is equal to QC = 5 and its Hardware complexity is HC = 3 α + 4 β + 2 δ [30].

N. Sayem Gate SG

A reversible gate 4 * 4 have as inputs A, B, C and D as outputs P = A, Q = A'B $\bigoplus$ AC, R = A'B $\bigoplus$ AC $\bigoplus$ D and S = AB $\bigoplus$ A'C $\bigoplus$ D. The quantum cost of the gate SG is equal to QC = 5 and its Hardware complexity is equal to HC = 4 α + 4 β + 1 δ [31].

III. Literature Review

We will present all the recent studies related to our proposed designs, starting by:

A. Design of the Converter from Decimal to BCD Encoder or D2BE

The decimal number system is made up of ten numbers from zero to nine to convert it in BCD Format, using a system called D2BE composed of ten inputs and four outputs. the inputs range from D0 to D9 and the outputs are A, B, C, and D [11] [12] [21] outputs are expressed depending on the inputs as follows:

A = D8 $\bigoplus$D9

B = D4 $\bigoplus$ D5 $\bigoplus$ D6 $\bigoplus$ D7

C = D2 $\bigoplus$ D3 $\bigoplus$ D6 $\bigoplus$ D7

D = D1$\bigoplus$D3 $\bigoplus$ D5 $\bigoplus$ D7 $\bigoplus$ D9

Table I presents the truth table of the converter from decimal to BCD encoder.

TABLE I. D2BE CONVERTER TRUTH TABLE

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A	B	C	D
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

The inputs of the converter from decimal to BCD encoder are: D9, D8, D7, D6, D5, D4, D3, D2, D1 and D0 and its outputs are:A,B,C and D.

We present below the related recent studies:

1) Design1: In 2012 JUN-CHAO WANGI [11] designed the converter from decimal to BCD encoder composed of five CNOT gates and fifteen Toffoli Gate gates (Fig. 1). According to the circuit proposed by JUN-CHAO WANGI, we have the performance criteria as follows:

-Number of gates: Its proposed circuit consists of five CNOT gates and 15 Toffoli gates. therefore CG = 20.

-Number of garbage outputs: As it indicated NGO = 25.

-Number of constant inputs: This criteria is not mentioned.

-Quantum cost: Its circuit is composed of five CNOT reversible gates having QC = 5 (QC = 1 for each) and fifteen TG reversible gates having QC = 75 (QC = 5 for each) therefore QC = 80.

-Hardware complexity: The circuit contains five CNOT reversible gates and fifteen TG reversible gates so HC =5α + 15(1α +1β) =20α+15β.

2) Design2 and Design3: In 2014 VANDANA SHUKLA [12] designed 2 designs of the decimal to BCD converter encoder which are as follows:

*Design2: This design is the circuit of the converter from decimal to BCD encoder design2 as shown in Fig. 2. According to this proposed circuit we have the performance criteria as follows:

-Number of gates: Its proposed circuit consists of 12 FG gates including four gates reversible TKS therefore CG = 16.

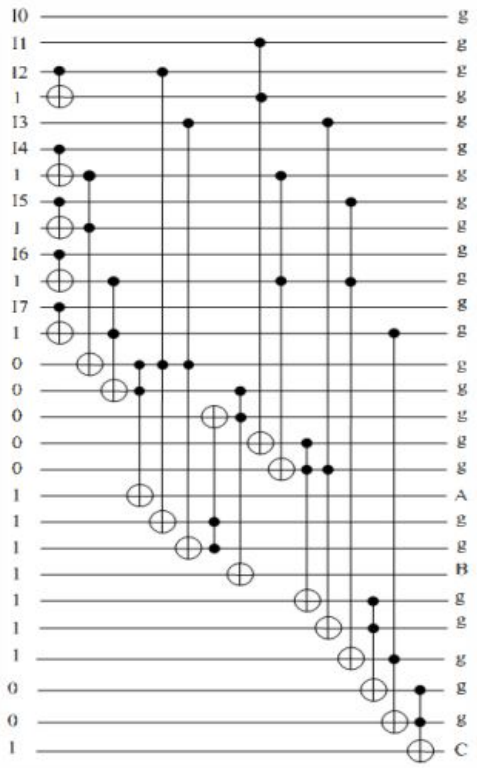

Fig. 1. Design1 D2BE.

-Number of garbage outputs: Proposed circuit consists of 12 FG gates including seven among they have one garbage output and four TKS reversible gates, each of which has two garbage outputs so NGO = 15.

-Number of constant inputs: Proposed circuit consists of 12 FG gates including two among them one constant entrance and four TKS reversible gates, each of which has one entrance constant therefore NCI = 6.

-Quantum cost: The quantum cost is not mentioned by VANDANA SHUKLA.

-Hardware complexity: The circuit contains 12 reversible gates FG and four TKS reversible gates so HC =12α + 4(2α +4β+1δ) =20α+16 β+4δ.

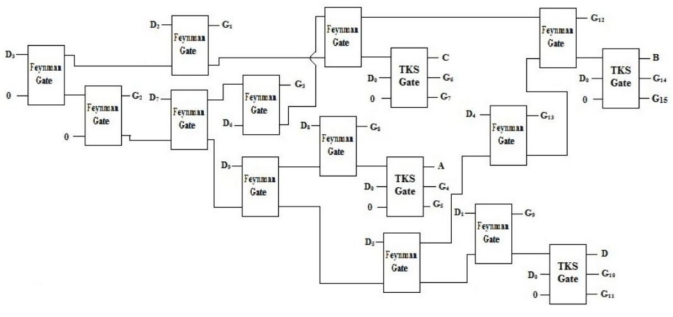

Fig. 2. Design2 D2BE.

*Design3: This design presents the decimal to BCD converter circuit design3 encoder (Fig. 3). According to this proposed circuit we have the performance criteria as follows:
-Number of gates: Its proposed circuit consists of 10 reversible BJN gates therefore CG = 10.

-Number of garbage outputs: Its proposed circuit consists of 10 BJN reversible gates of which six among them have two garbage output and three of them have one garbage output and one reversible gate BJN has no garbage output so NGO = 15.

-Number of constant inputs: The proposed circuit consists of 10 reversible gates BJN each of which has one constant input so NCI = 10.

-Quantum cost: The proposed circuit consists of 10 BJN reversible gates having QC = 50 (including QC = 5 for each) so QC = 50.

-Hardware complexity: The circuit contains 10 reversible gates BJN so HC =10α.

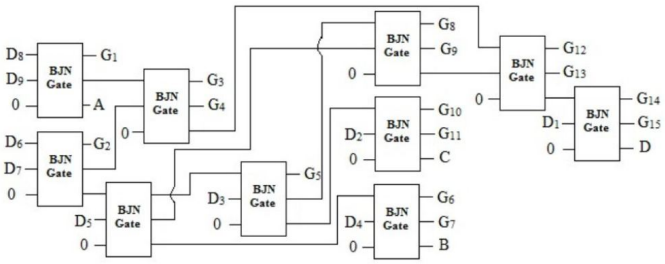

Fig. 3. Design3 D2BE.

3) Design4: In 2016 KUNAL CHAUDHARY [13] devised a design for the converter from decimal to BCD encoder is composed of four reversible gates Fredkin Gate FRG and three reversible gates FG in the following figure (Fig. 4). According to this proposed circuit we have the performance criteria as follows:

-Number of gates: CG = 11.

-Number of garbges outputs: NGO = 11.

-Number of constant inputs: NCI = 5.

-Quantum cost: QC = 23.

-Hardware complexity:The circuit contains 10 reversible gates Fredkin gate so HC =4(2α+4 β+1δ)+3α HC =11α+16 β+7δ.

4) Design5 et Design6: In 2019 SHEBA DIAMOND THABAH [14] devised two designs of the decimal converter to BCD encoder which are as follows:

*Design5: The decimal to BCD converter circuit design5 encoder as explained in Fig. 5. According to this proposed circuit we have the performance criteria as follows:
-Number of gates: Its proposed circuit consists of 10 reversible PG gates, of which therefore CG = 10.

-Number of garbage outputs: Its proposed circuit consists of 10 reversible PG gates of which five of them have two garbage output and five of them have one garbage output so NGO = 15.

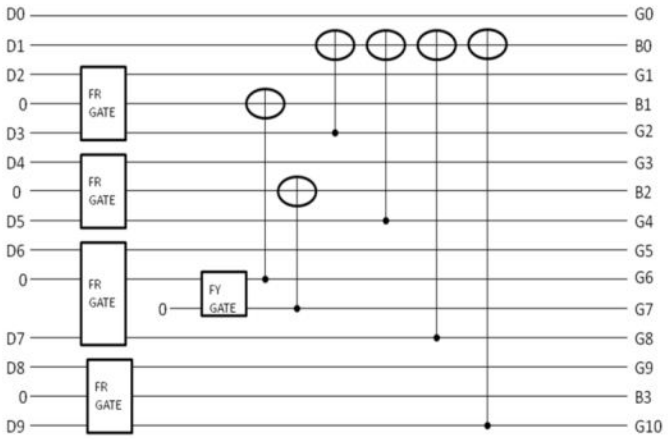

Fig. 4. Design4 D2BE.

-Number of constant inputs: Proposed circuit consists of 10 reversible PG gates of which nine of them has one constant input and the tenth has no constant input therefore NCI = 9.

- Quantum cost: Its proposed circuit consists of 10 reversible PG gates having QC = 40 (including QC = 4 for each) so QC = 40.

-Hardware complexity: The circuit contains 10 reversible gates Peres gate so: HC =10(2α+1 β) HC =20α+10 β

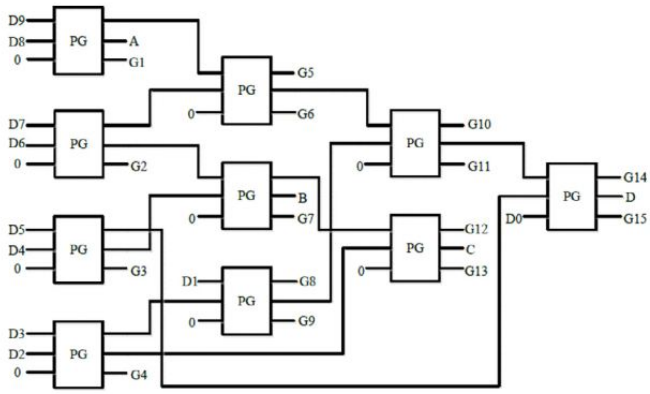

Fig. 5. Design5 D2BE.

*Design6: The decimal to BCD converter circuit design6 encoder (Fig. 6). According to this proposed circuit, we have the performance criteria as follows:

-Number of gates: Its proposed circuit consists of 11 FG reversible gates therefore CG = 11.

-Number of garbage outputs: Its proposed circuit consists of 10 FG reversible gates of which five of them have one garbage output and one of them has two garbage outputs and five among them has no garbage output so CG = 7.

-Number of constant inputs: Its proposed circuit consists of 10 reversible gates FG of which one gate among them has one constant input and the others have no constant input therefore NCI = 1.

-Quantum cost: Its proposed circuit consists of 11 FG reversible gates having QC = 11 (including QC = 1 for each) so QC = 11.

-Hardware complexity: The circuit contains 11 reversible gates of Feyman gate so HC =11(1α) HC =11α

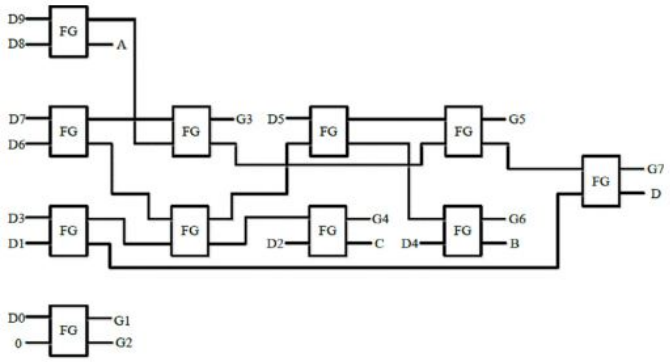

Fig. 6. Design6 D2BE.

B. Design of Reversible Binary Counter with Up/Down

It is a binary counter counting from 0 to 15 using a clock and which is linked with an up / down button that after having the impulse the counting becomes a countdown. In the following, we present the recent studies making the design of this type of binary counter.

1) Design1: IN 2016 Xuemei Q [15] proposed a design of the reversible binary counter (Fig. 7) as follows: the TFF gate is equivalent to the TFG and FG gate according to the circuit below (Fig. 8). Then based on the above we can present the performance criteria of this circuit as follows:

-Number of gates: Its proposed circuit consists of four TFF reversible gates, six gates reversible PG, three reversible gates MTG and one reversible gate FG so CG = 14.

-Number of garbage outputs: Its proposed circuit consists of three TFF reversible gates each having one garbage output, one TFF reversible gate with three garbage outputs, three reversible PG gates with one garbage output for each, three reversible PG gates with two garbage outputs for each, two reversible MTG gate with two garbage outputs for each and none of the FG reversible gates has a garbage output so NGO = 17.

-Number of constant inputs: This circuit consists of four TFF reversible gates each having two constant inputs, six reversible PG gates having one constant input for each, three MTG reversible gates with one constant inputs for each, one reversible gate FG having one constant input so NCI = 18.

-Quantum cost: Its proposed circuit consists of four TFF reversible gates having QC=24 (each of TFF composed of one TFG and one FG then we have QC (TFF) = 6 because we have QC (TFG) = 5 and QC (FG) = 1), six reversible gates PG having QC = 24 (QC = 4 for each), three MTG reversible gates having QC = 15 (QC = 5 for each), one reversible gate FG having QC = 1 therefore QC = 64.

-Hardware complexity: Its proposed circuit consists of four TFF reversible gates having HC = 16α + 4β (each of which HC = 4α + 1β because we have HC (TFG) = 3α + 1β and HC (FG) = 1α), six reversible gates PG with HC = 12α + 6β (HC = 2α + 1β for each), three reversible gates MTG having HC = 3α (each of which HC = 1α), and one reversible gate FG having HC = 1α therefore HC = 32α + 10β.

2) Design2: In 2011 V. Rajmohan [16] proposed a design of the reversible binary counter as follows (Fig. 9):

The TFF reversible gate is equivalent to the circuit below (Fig. 10). The performance criteria of this circuit as follows:

-Number of gates: The proposed circuit consists of four gates reversible TFF (each of which is made up of two SG reversible gates and one reversible gate FG), three reversible gates FRG, three reversible gates RSJ therefore CG = 18.

-Number of garbage output: Its proposed circuit consists of four TFF reversible gates, each of which has three garbage outputs (because a TFF consists of two reversible SG gates, the first gate has one garbage output and the second has two outputs and the FG gate does not have no garbage output), and the fourth gate has one more garbage output, three reversible gates RSJ each of then has one garbage output, three reversible FRG gates including two among they have one garbage output and the third has two garbage outputs so NGO = 20.

-Number of constant inputs: Its proposed circuit consists of four TFF reversible gates each having two constant inputs, six reversible PG gates having one constant input for each, three MTG reversible gates with one constant inputs for each, one gate reversible FG having one constant input so NCI = 23.

-Quantum cost: Its proposed circuit is made up of 4 reversible gates TFF having QC = 44 (because a TFF is made of two gates reversible SG and one gate FG then QC = 11), three reversible gates RSJ having QC = 36 (including each having QC = 12), three FRG reversible gates having QC = 15 (each having QC = 5) and a NOT gate we took it into consideration so QC = 96. -Hardware complexity: the proposed circuit consists of four TFF reversible gates having HC = 36 α + 32 β + 8 δ (because a TFF consists of two reversible SG gates having HC = 8 α + 8 β + 2 δ and a FG gate then HC = 1 α), three reversible gates RSJ having HC = 6 α + 3 β (each of which having HC = 2 α + 1 β), three FRG reversible gates having HC = 6 α + 12 β + 3 δ (each having HC = 2 α + 4 β + 1 δ) and a NOT bear it has been taken into consideration HC = 1 δ so HC = 48 α + 47 β + 12 δ.

3) Design3: In 2019 Mubin Ul Haque [17] proposed a design of the reversible binary counter (Fig. 11) as following:

We can present the performance criteria of this circuit as follows:

-Number of gates: Its proposed circuit consists of four reversible MSH gates, three gates reversible HNG, and one reversible gate TS-3 and a NOT gate therefore CG = 9.

-Number of garbage outputs: Its proposed circuit consists of four MSH reversible gates each of which has two garbage outputs, three HNG reversible gates, each of which has one constant input, and one reversible gate TS-3 having no constant input so NGO = 16.

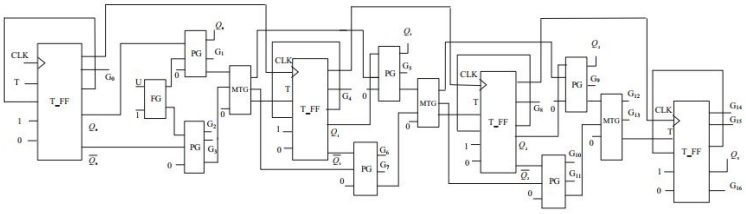

Fig. 7. Design1 Reversible 4-bit Controlled Up/Down Synchronous Counter.

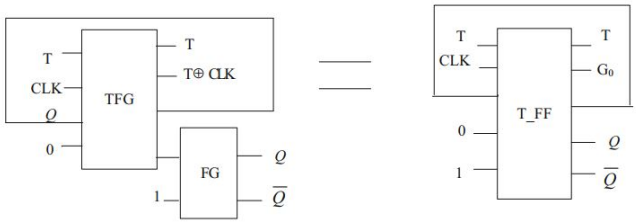

Fig. 8. Block of Reversible T Flip-flop.

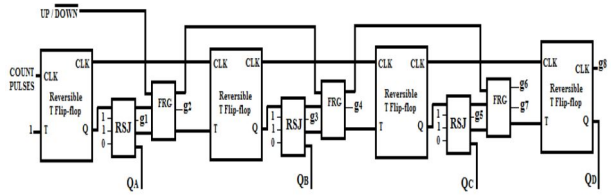

Fig. 9. Design2 Reversible 4-bit Controlled Up/Down Synchronous Counter.

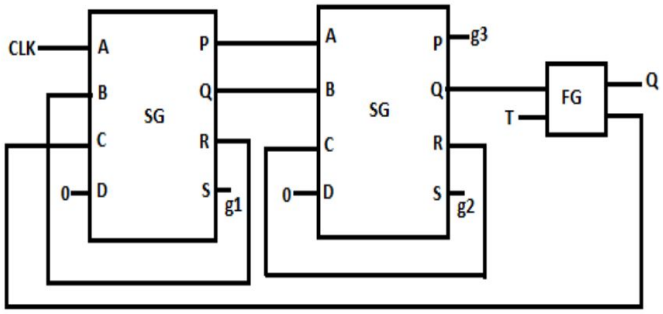

Fig. 10. Equivalent Circuit of T Flip-flop.

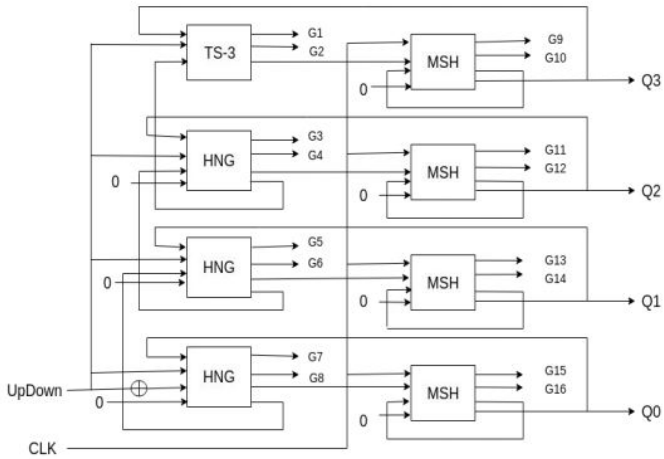

Fig. 11. Design3 Reversible 4-bit Controlled Up/Down Synchronous Counter.

-Number of constant inputs: Its proposed circuit consists of four MSH reversible gates each of which has two constant inputs, three HNG reversible gates, each of which has two garbage outputs, and one reversible TS-3 gate with two garbage outputs so NCI = 7.

-Quantum cost: Its proposed circuit consists of four MSH reversible gates having QC = 24 (of which having QC = 6), three reversible gates HNG having QC = 18 (each of which having QC = 6) and one reversible gate TS-3 QC = 2 therefore QC = 44.

-Hardware complexity: Its proposed circuit consists of four reversible MSH gates having HC = 12 α + 8 β + 4 δ (each having HC = 3 α + 2 β + 1 δ), 3 HNG reversible gates having HC = 12 α + 6 β (each having HC = 4 α + 2 β) and one reversible gate TS-3 HC = 2 α and one NOT gate having HC = 1 δ so HC = 26 α + 14 β + 5 δ.

Limitations of previous studies: We find in these previous studies a certain limitation in terms of less optimized performance criteria, the proof is that we were able to make our designs with better performance criteria than the previous works while keeping the same functionality.

IV. Our Proposed Designs

In this section, we will present our design of the converter from Decimal to BCD encoder, which we will be interested in obtaining the functional outputs which are:

A = D8 $\bigoplus$ D9
B = D4 $\bigoplus$ D5 $\bigoplus$ D6 $\bigoplus$ D7
C = D2 $\bigoplus$ D3 $\bigoplus$ D6 $\bigoplus$ D7
D = D1$\bigoplus$D3 $\bigoplus$ D5 $\bigoplus$ D7 $\bigoplus$ D9
Our design is consisting of five HNFG reversible gates. Fig. 12 present our proposed circuit and its performance criteria:

* Number of gates: We have five reversible gates of the HNFG so CG = 5.

* Number of garbage outputs: Our design has the same functional outputs showed above. Concerning the garbage outputs, based on the functions of the reversible gates are as follows: G1 = D9, G2 = D1, G3 = D5, G4 = D9$\bigoplus$D7, G5 = D7$\bigoplus$D6 Then NGO = 5.

* Number of constant inputs: We notice that there is no

constant input therefore NCI = 0.

* Quantum cost: We have five reversible gates of the HNFG so QC = 10 (QC = 2 for each gate).

-Hardware complexity: The proposed circuit consists of five reversible HNFG gates having HC = 10 α (each of which having HC = 2 α).

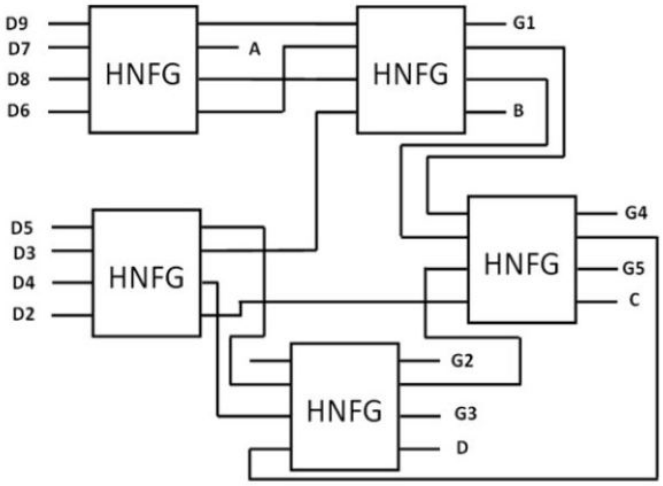

Fig. 12. Our Design of the Converter from Decimal to BCD Encoder orD2BE.

And in the other hand, we will present our proposed circuit of the reversible binary counter by showing its performance criteria while revealing the improvement percentages in terms of these parameters compared to three recent designs. Based on the circuit of [17], we replace the reversible gate MSH by the reversible gate NP since they have the same functional outputs (third and fourth output) if we fix the fourth entry by 0, by the following, we obtain below our circuit (Fig. 13). Then based on our proposed design we can present the performance criteria of this circuit as follows:

-Number of gates: Its proposed circuit consists of four NP reversible gates, three reversible gates HNG, and one reversible gate TS-3 and a NOT gate therefore CG = 9.

-Number of garbage outputs: The proposed circuit consists of four NP reversible gates each of which has two garbage outputs, three HNG reversible gates, each has one constant input, and one reversible gate TS-3 having no constant input so NGO = 16.

-Number of constant inputs: The proposed circuit consists of four NP reversible gates each of which has two constant inputs, three HNG reversible gates, each of which has two garbage outputs, and one reversible TS-3 gate with two garbage outputs so NCI = 7.

-Quantum cost: the proposed circuit consists of four NP reversible gates having QC = 20 (of which having QC = 5), three reversible gates HNG having QC = 18 (each of which having QC = 6) and one reversible gate TS-3, QC = 2; therefore QC = 40.

-Hardware complexity: The proposed circuit consists of four NP reversible gates having HC = 12α + 16β + 8δ (each of which having HC = 3α + 4β + 2δ), three reversible gates HNG having HC = 12α + 6β (each of which has HC = 4α + 2β) and one reversible gate TS-3 HC = 2α and one NOT gate having HC = 1δ so HC = 26α + 22β + 9δ.

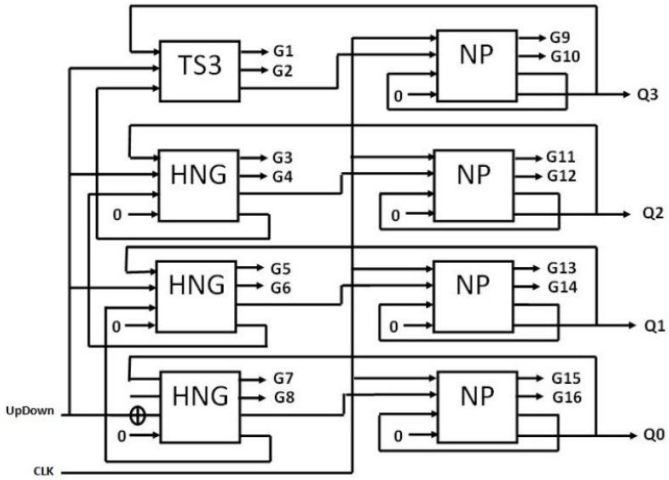

Fig. 13. Our Design of Reversible Binary Counter with Up/ Down.

V. Results and Discussion

So in this section, we will compare our results obtained compared to recent studies of the D2BE converter circuit and those of the reversible binary counter.

Regarding the first circuit, we will draw up a comparative table, that is, Table II showing performance criteria.

TABLE II. Comparative Table of Performance Criteria for Recent Designs of D2BE and our Improvements Obtained

Circuit D2BE	CG	NGO	NCI	QC	HC
Our design	5	5	0	10	10α
Expolited design1 [11]	20	25	—	80	20α + 15β
Expolited design2[12]	16	15	6	—	20α + 16β + 4δ
Expolited design3[12]	10	15	10	50	10α
Exploited design4[13]	11	11	5	23	11α + 16β + 4δ
Exploited design5 [14]	10	15	9	40	20α + 10β
Exploited design6[14]	11	7	1	11	11α
%Imp (Design1)[11]	75	80	—	87,5	50CNOT ,100AND
%Imp (Design2) [12]	68,75	66,67	100	—	50CNOT, 100AND 100NOT
%Imp (Design3)[12]	50	66,67	100	80	no improvement is obtained
%Imp (Design4)[13]	54,54	54,54	100	56,52	9,09CNOT,100AND , 100NOT
%Imp (Design5)[14]	50	66,67	100	75	50CNOT 100AND
%Imp (Design6)[14]	54,54	28,57	100	9,09	9,09CNOT

So in this section, we will compare our results obtained compared to recent studies of the D2BE converter circuit and those of the reversible binary counter.

For the design:

-Design1 [11]: 75%, 80%, 87.5% ,50%, 100% in terms of CG, NGO, QC, CNOT, ND, respectively. -Design2 [12]: 68.75%, 66.67%, 100%, 50%, 100%, 100% in terms of CG, NGO, NCI, CNOT, AND, NOT, respectively.
-Design3 [12]: 50%, 66.67%, 100%, 80% in terms of CG, NGO, NCI, QC, AND, respectively.

-Design4 [13]: 54.54%, 54.54%, 100%, 56.52%, 9,09%, 100%, 100% in terms of CG, NGO, NCI, QC, CNOT, AND, NOT, respectively. -Design5 [14]: 50%, 66.67%, 100%, 75% and 50%, 100% in terms of CG, NGO, NCI, QC, CNOT, AND, respectively.
-Design6 [14]: 54.54%, 28.57%, 100%, 9.09%, 9.09% in terms of CG, NGO, NCI, QC, CNOT Deadline, respectively.

We will present the following graph of performance criteria of D2BE designs shown in Fig. 14.

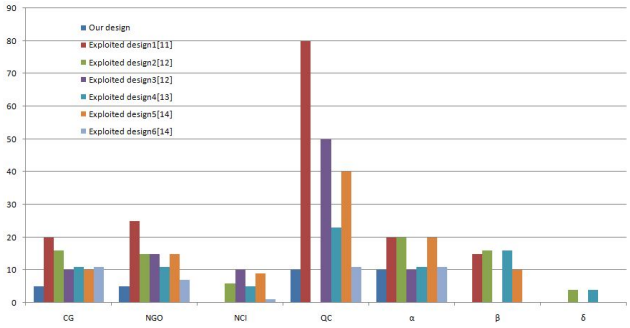

Fig. 14. Performance Criteria of D2BE Designs.

Then concerning the reversible binary counter circuit and According to the recent designs mentioned below and their performance criteria and according to our proposed design we can draw up the following comparative table (Table III).

TABLE III. COMPARATIVE TABLE OF PERFORMANCE CRITERIA FOR RECENT DESIGNS OF REVERSIBLE BINARY COUNTER WITH UP/ DOWN AND OUR IMPROVEMENTS OBTAINED

Binary reversible counter	CG	NGO	NCI	QC	HC
Our design	9	16	7	40	$26\alpha+22\beta+9\delta$
Exploited Design 1 [15]	14	17	18	64	$32\alpha+10\beta$
Exploited Design2 [16]	18	20	23	96	$48\alpha+47\beta+12\delta$
Exploited Design3 [17]	9	16	7	44	$26\alpha+14\beta+5\delta$
%Imp [15]	35,71	5,88	61,11	37,5	18,75 CNOT
%Imp [16]	50	20	69,56	58,33	45,83 CNOT,53,19AND et 25 NOT
%Imp [17]	—	—	—	9,09	no improvement is obtained

According to this table we were able to improve the performance criteria in our proposed design compared to six recent designs as follows: For the design:

-Design1 [15]: 35.71%, 5.88% and 61.11%, 37.5%, 18.75% in terms of CG, NGO, NCI, QC, number of CNOT gates, respectively.

-Design2 [16]: 50%, 20% and 69.56%, 58.33%, 45.83%, 53.19%, 25% CG, NGO, NCI, QC, number of CNOT gates, number of CNOT gates number of AND gates and number, number of NOT gates. NOT gates, respectively.

-Design3 [17]: 9.09% in terms of QC.

According to these results obtained, they are represented in the graph below (Fig. 15).

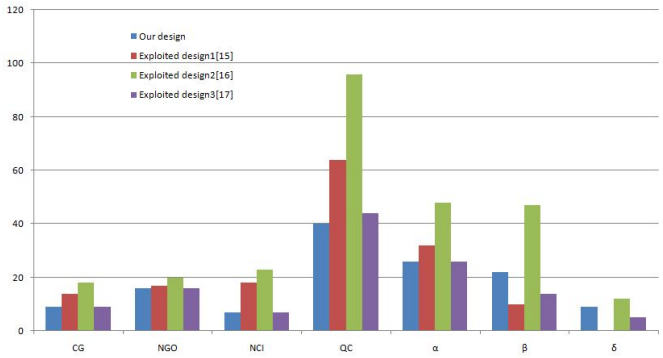

Fig. 15. Performance Criteria of Reversible 4-bit Controlled Up/Down Synchronous Counter Design.

VI. CONCLUSION

Reversible logic occupies a significant role in reducing energy loss at the end of unused bits in the circuit compared to conventional logic computation. Our design was able to minimize all performance criteria especially the number of garbage outputs in our D2BE circuit and the reversible binary counter,as a result a decrease in the energy dissipated at the end of unused bits because heat is directly related to fewer garbage outputs, therefore our designs are adequate for low power application. We show also an improvement in terms of other performance criteria exposing remarkable results. While waiting for new reversible gates to exploit in the future, we can optimize the D2BE circuit and that of the reversible binary counter respecting the performance, typically concerning minimizing heat energy.

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