Effect of Driver Strength on Crosstalk in Global Interconnects

Kalpana.A.B
Assistant Professor,
Department of Electronics and Communication
Bangalore Institute of Technology
Bangalore, India

P.V.Hunagund
Professor
Department of Applied Electronics
Gulbarga University
Gulbarga, India

***Abstract*— The Noise estimation and avoidance are becoming critical, in today's high performance IC design. An accurate yet efficient crosstalk noise model which contains as many driver/interconnect parameters as possible, is necessary for any sensitivity based noise avoidance approach. In this paper, we present an analysis for crosstalk noise model which incorporates all physical properties including victim and aggressor drivers, distributed RC characteristics of interconnects and coupling locations in both victim and aggressor lines. Also shown that crosstalk can be minimized by driver sizing optimization technique. These models are verified for various deep submicron technologies.**

Keywords- Coupling; crosstalk; Interconnect; noise; victim.

I. INTRODUCTION

Coupling capacitance between neighboring nets is a dominant component in today's deep submicron designs as taller and narrower lines are being laid out closer to each other [1]. This trend is causing the ratio of crosstalk capacitance to the total capacitance of a wire to increase. On top of these interconnect related trends, more aggressive and less noise immune circuit structures such as dynamic logic are being employed more commonly due to performance requirements.

As a result, a significant crosstalk noise problem exists in today's high performance designs. The net on which noise is being induced is called the *victim* net whereas the net that induces this noise is called the *aggressor* net. Crosstalk noise not only leads to modified delays [2, 3] but also to potential logic malfunctions [4, 5]. To be able to deal with the challenges brought by this recently emerging phenomenon, techniques and tools to estimate and avoid crosstalk noise problems should be incorporated into the IC design cycle from the early stages. Any such tool requires fast yet accurate crosstalk noise models both to estimate noise and also to see the effects of various interconnect and driver parameters on noise. Several papers, which propose crosstalk models, can be found in recent literature. In [6], telegraph equations are solved directly to find a set of analytical formulae for peak noise in capacitively coupled bus lines. [7] derives bounds for crosstalk noise using a lumped model but assuming a step input for aggressor driver. The peak noise expression in [7] is extended by [8, 9] to consider a saturated ramp input and a π circuit to represent the interconnect. These models fail to represent the distributed nature of the interconnect. In [10], an Elmore delay like peak noise model is obtained for general RC trees but it assumes an infinite ramp input. This assumption causes the model to significantly overestimate peak noise, especially for small aggressor slews, which is very likely to occur in today's deep submicron designs. Devgan's metric has been improved in [11]. Interconnect crosstalk can be modeled and minimized using different techniques [12, 13] It is also shown that crosstalk can be minimized by driver sizing optimization technique [14, 15].

II. NOISE AVOIDANCE TECHNIQUE: DRIVER SIZING

A general case for two coupled lines is shown in Figure 1. Both aggressor and victim lines are divided into 3 regions: interconnect segment before coupling location, coupling location and interconnect segment after coupling location. These regions of aggressor and victim lines are represented by L_{al}, L_c, L_{ar}, L_{vl} and L_{vr} as seen in the figure 3. We propose the linear model shown in Figure 4 to compute crosstalk noise at the receiver of victim net. Victim driver is modeled by effective holding resistance R_h whereas aggressor driver is modeled by an effective Thevenin model consisting of a saturated ramp voltage source with a slew rate of t_r and the Thevennin resistance R_{th}. Other components of our model are computed based on the technology and geometrical information obtained from Figure 1. Coupling node (node 2 in aggressor net and node 5 in victim net) is defined to be the middle of coupling location for both nets, i.e. $L_{al} + L_c/2$ away from aggressor driver and $L_{vl} + L_c/2$

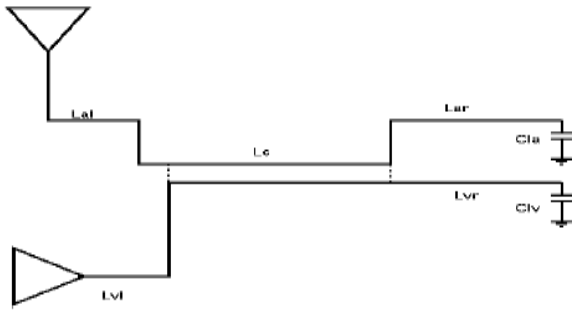

Figure 1. Linear crosstalk noise model

away from the victim driver. For the aggressor net, let the upstream and downstream resistance-capacitance at node 2 be R_{a1}-C_{au} and R_{a2}-C_{ad} respectively. Then, $C_{a1} = C_{au}/2$, Ca2 = $(C_{au}+C_{ad})/2$ and $C_{a3} = C_{ad}/2+C_{la}$. Similarly for the victim net, let the upstream and downstream resistance capacitance pair at

node 5 be R_{v1}-C_{vu} and R_{v2} -C_{vd} respectively. Then, $C_{v1} = C_{vu}/2$, $C_{v2} = (C_{vu} + C_{vd})/2$ and $C_{v3} = C_{vd}/2 + C_{lv}$.

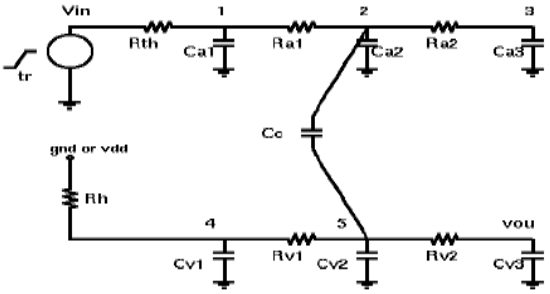

Figure 2. Linear crosstalk noise model

To simplify the analytical calculation of transfer function H(s) from V_{in} to V_{out}, we initially decouple the aggressor line from victim line (Figure 3 (a)), and compute the transfer function from V_{in} to V_2. We then apply $V_2(s)$ to the victim line as seen in Figure 3 (b). This assumption is valid when victim line is not loading aggressor line at node 2 significantly.

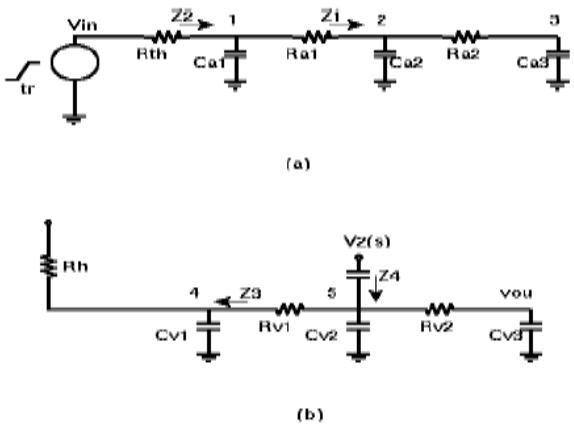

Figure 3. Decoupled model to calculate transfer Function.

We will look at driver sizing both from the point of view of victim driver sizing and aggressor driver sizing. Intuitively, if a victim driver is sized up, its effective conductance increases thus it becomes stronger to hold a net at a steady voltage (V_{dd} or ground). On the other hand, if an aggressor driver is sized down, its effective conductance decreases thus it cannot transition as fast and as a result noise amount that it can induce on a victim net decreases. Victim driver is modeled by effective holding resistance R_h whereas aggressor driver is modeled by an effective Thevenin model consisting of a saturated ramp voltage source with a slew rate of t_r and the Thevenin resistance R_{th}. Using our model, we have calculated the sensitivity of peak noise to R_h and

R_{th} which represent victim and aggressor driver sizes, respectively.

$$\frac{\delta_{vpeak}}{\delta R_h} = \frac{C_C}{t_r}\left(1 - e^{-t_r/t_v}\right) - \left(R_h + R_{v1}\right)\frac{C_C\left(C_C + C_{v1} + C_{v2} + C_{v3}\right)}{t_v^2} e^{-t_r/t_v} \qquad (15)$$

$$\frac{\delta v_{peak}}{\delta R_{th}} = \frac{-\left(R_h + R_{v1}\right)C_C\left(C_{a1} + C_{a2} + C_{a3}\right)}{t_v^2} e^{-t_r/t_v} \qquad (16)$$

Since Equation (16) is always negative, sizing down the aggressor driver (i.e., sizing up R_{th}) will always reduce peak noise. But how effective a reduction it will be, depends on the parameters of Equation (16). Increasing R_{th} will be more effective on noise reduction if the numerator of Equation (16) is greater than its denominator.

If the equation parameters are carefully observed, this mathematical condition translates to the following circuit condition. Noise reduction effect of increasing R_{th} is more, when we have a strong aggressor (strong aggressor driver, wide/short aggressor line). The effects of sizing up victim driver (i.e.sizing down R_h) is more complicated. In terms of peak noise reduction, victim driver sizing becomes a more effective noise avoidance tool as the RC time constant of victim line decreases.

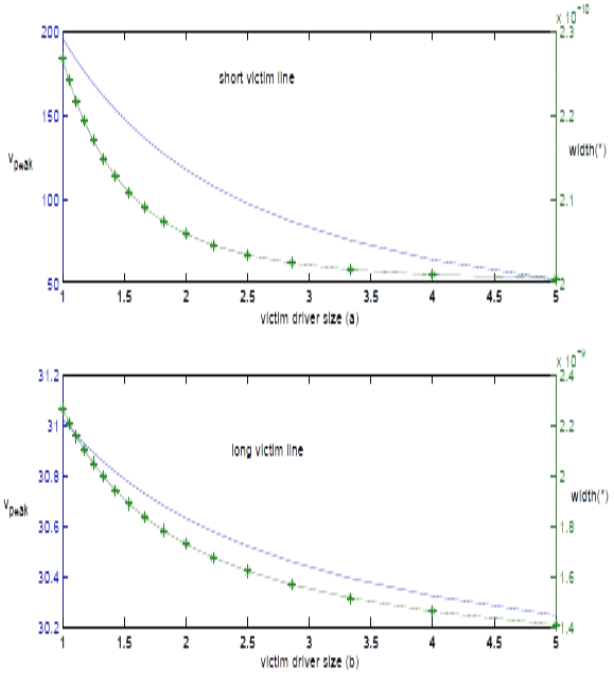

Figure 4. Sensitivity of victim driver sizing effects to victim line properties

Figure 4(a) shows the effects of victim driver sizing on a short victim line. Note that peak noise voltage is reduced by 75mV/38.5% whereas noise width is reduced by 22ps/9.6% when victim driver size is doubled. As RC time constant of victim line increases, victim driver sizing becomes less effective in terms of peak noise reduction but it is important to notice the effects on noise width.

As seen in Figure 6(b), victim driver sizing on a long victim line reduces noise width by 550ps/24% while peak noise is reduced by 0.4mV/1% when victim driver size is doubled. One other important observation about victim driver sizing is the diminishing returns effect.

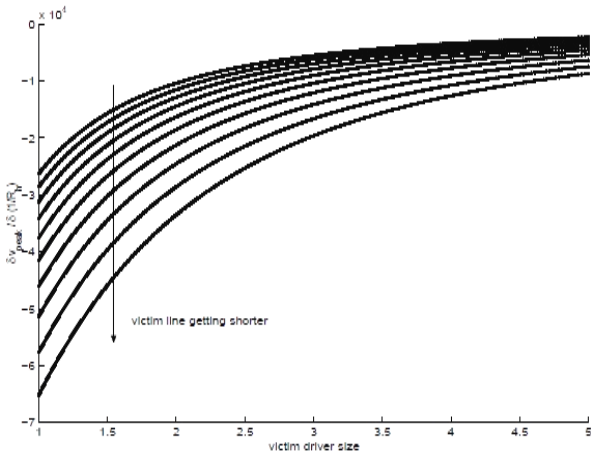

Figure 5. Diminishing returns effect in victimdriver sizing.

Figure 5 shows change in $\delta v_{peak}/\delta(1/R_h)$ as victim driver is sized up, for a range of victim line lengths. As can be seen, the effect of driver sizing diminishes as victim driver is sized up. A driver sizing tool should take this effect into account to be able to steer away from non-optimal sizes and to make sure that the area trade-off is worthwhile.

III. RESULTS

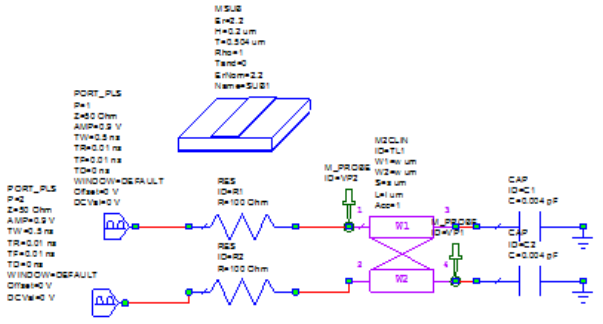

Figure 6. Experimental circuit using AWR

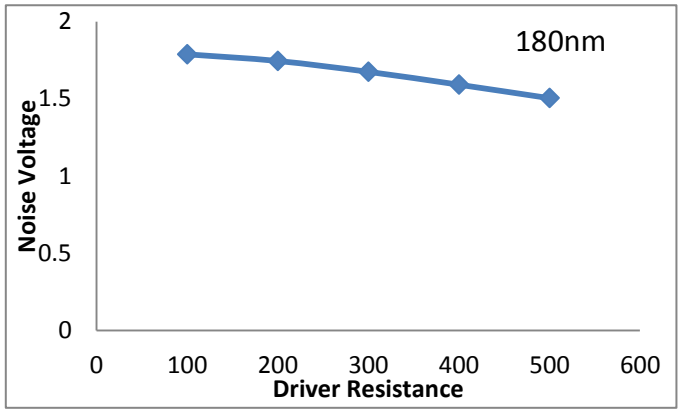

Figure 7. Noise voltage with change in driver resistance for 180 nm

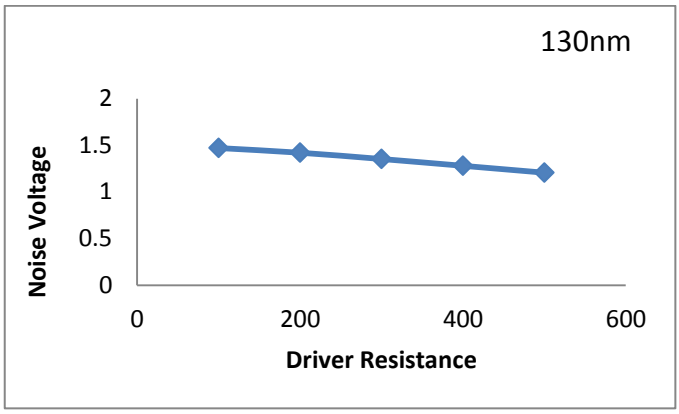

Figure 8. Noise voltage with change in driver resistance for 130 nm

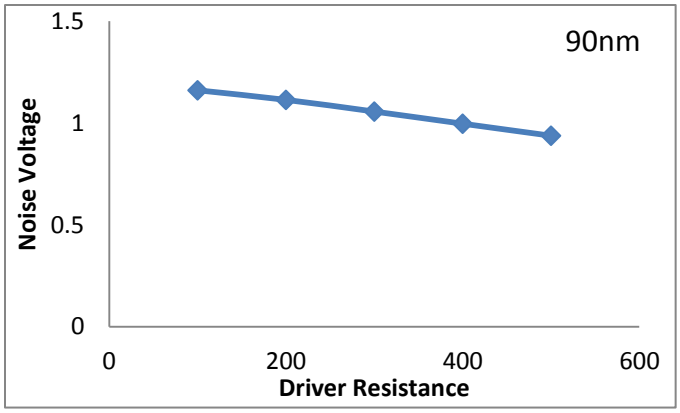

Figure 9 Noise voltage with change in driver resistance for 90 nm

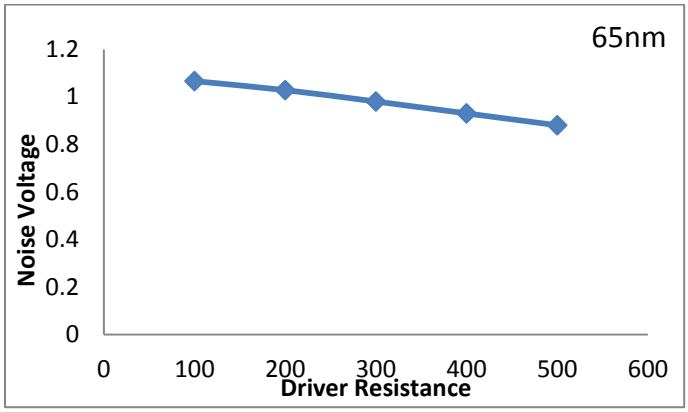

Figure 10. Noise voltage with change in driver resistance for 65nm

Figure 6. shows the experimental setup used for simulation in AWR software.

Figure 7.to figure 11. Shows the variation in crosstalk noise voltage with the change in driver resistance for different technology nodes.

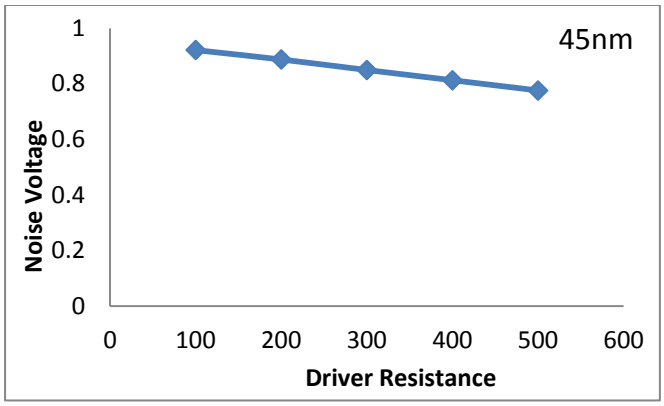

Figure 11. Noise voltage with change in driver resistance for 45nm

III. CONCLUSION

In this paper, we presented analysis for crosstalk noise model which incorporates all victim and aggressor driver/interconnect physical parameters including coupling locations on victim and aggressor nets, distributed RC characteristics of interconnects. Crosstalk noise minimization technique using driver sizing also developed and validated for deep submicron technologies. Output voltage is observed for increased driver size and shown that crosstalk can be minimized by driver optimization.

REFERENCES

[1]. S. I. Association. The international technology roadmap for semiconductors, 1999.

[2]. P. D. Gross, R. Arunachalam, K. Rajagopal, and L. T. Pileggi. Determination of worst-case aggressor alignment for delay calculation. In Proceedings of the IEEE International Conference on Computer-Aided Design, ICCAD-98, 1998.

[3]. S. Sirichotiyakul, D. Blaauw, C. Oh, R. Levy, V. Zolotov, and J. Zuo. Driver modeling alignment for worst-case delay noise. In Proceedings of Design Automation Conference DAC, pages 720–725, June 2001.

[4]. S. Alwar, D. Blaauw, A. Dasgupta, A. Grinshpon, R. Levy, C. Oh, B. Orshav, S. Sirichotiyakul, and V. Zolotov. Clarinet: A noise analysis tool for deep submicron design. In Proceedings of Design Automation Conference DAC, pages 233–238, June 2000.

[5]. K. L. Shepard and V. Narayanan. Noise in deep submicron digital design. In Proceedings of ICCAD-96 Intl. Conference on Computer Aided Design, pages 524–531, November 1996.

[6]. T. Sakurai. Closed-form expression for interconnect delay, coupling, and crosstalk in VLSIs. IEEE Transactions on Electron Devices, 40:118–124, 1993

[7]. A. Vittal and M. Marek-Sadowska. Crosstalk reduction for VLSI. IEEE Transactions on Computer Aided Design, 16:290–298, March 1997.

[8]. A. Vittal, L. H. Chen, M. Marek-Sadowska, K. P. Wang, and S. Yang. Crosstalk in VLSI interconnections. IEEE Transactions on Computer Aided Design, 18:1817–1824, December 1999.

[9]. A. B. Kahng, S. Muddu, and D. Vidhani. Noise and delay uncertainty studies for coupled rc interconnects. In Proceedings of ASIC/SOC Conference, pages 3–8, 1999.

[10]. A. Devgan. Efficient coupled noise estimation for on-chip interconnects. In Proceedings of the IEEE International Conference on Computer-Aided Design, ICCAD-97, pages 147– 153, 1997.

[11]. M. Kuhlmann and S. S. Sapatnekar. Exact and efficient crosstalk estimation. IEEE Transactions on Computer Aided Design, 20(7):858–866, July 2001.