Hardware Segmentation on Digital Microscope Images for Acute Lymphoblastic Leukemia Diagnosis Using Xilinx System Generator

Prof. Kamal A. ElDahshan
Professor of Computer Science, Dept. of Mathematics,
Faculty of Science,
AL-AZHAR University, Cairo, Egypt

Prof. Mohammed I. Youssef
Dept. of Electronic Engineering, Faculty of Engineering,
AL-AZHAR University, Cairo, Egypt

Dr. Emad H. Masameer
Assistant Professor of Computer Science, Dept. of Mathematics, Faculty of Science,
AL-AZHAR University, Cairo, Egypt

Mohammed A. Mustafa
Lecturer assistant, Dept. of Management Information Systems, Modern Academy for Computer Science and Information Technology, Cairo, Egypt

***Abstract*—Image segmentation is considered the most critical step in image processing and helps to analyze, infer and make decisions especially in the medical field. Analyzing digital microscope images for earlier acute lymphoblastic leukemia diagnosis and treatment require sophisticated software and hardware systems. These systems must provide both highly accurate and extremely fast processing of large amounts of image data. In this work, the hardware segmentation framework for Acute Lymphoblastic Leukemia (ALL) images based color histogram of Hue channel of HSV color space is proposed to segment each leukemia image into blasts and background using Field Programmable Gate Array (FPGA). The main purpose of this work is to implement image segmentation framework in a FPGA with minimum hardware resources and low execution time to be suitable enough for medical applications. Hardware framework of segmentation is designed using Xilinx System Generator (XSG) as DSP design tool that enables the use of Simulink models, implemented in VHDL and synthesized for Xilinx SPARTAN-3E Starter kit (XC3S500E-FG320) FPGA.**

Keywords—Medical Image Processing; FPGA; Image Segmentation; Xilinx System Generator

I. INTRODUCTION

Leukemia is a type of cancer caused by abnormal increase of the white blood cells. According to [1] leukemia can be classified into acute and chronic. Acute leukemia spreads very rapidly and has to be treated promptly rather than chronic leukemia that does not have to be treated promptly. Acute leukemia can be either lymphoblastic (ALL) or myelogenous (AML), based on affected cell type. Chronic leukemia can be either lymphoblastic (CLL) or myelogenous (CML). Acute lymphoblastic leukemia (ALL) is considered the prime focus of this work, which has a higher expectation of survival rate compared to AML.

Image segmentation is a process of partitioning the image into multiple segments. For biomedical imaging applications, image segmentation is a founding step in image analysis as it will directly affect the post-processing. It is a crucial component in diagnosis [2] and treatment [3]. The main goal of acute leukemia blood cell segmentation is to extract components such as blast from its complicated blood cells background. There are many techniques that have been developed for image segmentation such as threshold techniques [4], edge detection [5] and watershed techniques [6]. Due to the complex nature of blood cells and overlapping between these cells, segmenting them remains a challenging task [7]. Many algorithms for segmentation have been developed for grayscale images rather than color images which require more information to be processed [8].

Image processing algorithms implemented in FPGA hardware have emerged as the most viable solution for improving the performance of image processing systems. It offers a compromise between the flexibility of general purpose processors and ASICs. FPGAs are recently used in many image processing applications such as image compression [9] [10] [11], image filtering [12] [13] and wireless communication [14] [15].

Xilinx System Generator is a DSP design tool [16] [17] that deal with many images processing application. XSG is a part of the ISE design suite that provides Xilinx DSP Blockset for application specific design. The main advantage of using Xilinx system generator for FPGA implementation is that Xilinx Blockset provides close integration with MATLAB Simulink that helps in co-simulating the FPGA module with pixel vector provided by MATLAB Simulink Blocks [18].

In this paper, segmentation based color histogram of Hue channel of HSV color space is used [19]. Before hardware segmentation, pre-processing of the acute lymphoblastic leukemia image to convert an image from RGB color space to HSV color space is required. This work focuses on implementing multilevel thersholding segmentation based on color histogram of H channel of HSV color space in hardware.

All algorithms are initially implemented in MATLAB to realize the segmentation results. The pipelined framework of

multilevel thersholding image segmentation is implemented in a FPGA. This work presents segmentation framework using Xilinx System Generator and also implemented in low cost basic FPGA device Spartan-3E.

II. Leukemia Segmentation

The ultimate goal of ALL segmentation is to extract components such as blast from its complicated blood cells background. There are 6 steps involved in applying image segmentation process:

Step 1: transforming the source RGB color space to HSV color space.

Step 2: extracting H channel from HSV color space.

Step 3: Selecting color range of nucleus and cytoplasm by using color histogram of H channel. Two angle values A1, A2 are obtained from color histogram for multilevel thersholding segmentation.

Step 4: Implementing the median filter N X N (N = 7) to the resulted images.

Step 5: Synthesizing the HSV image.

Step 6: Converting the HSV image to RGB to display.

Fig. 1 illustrates the block diagram of ALL segmentation.

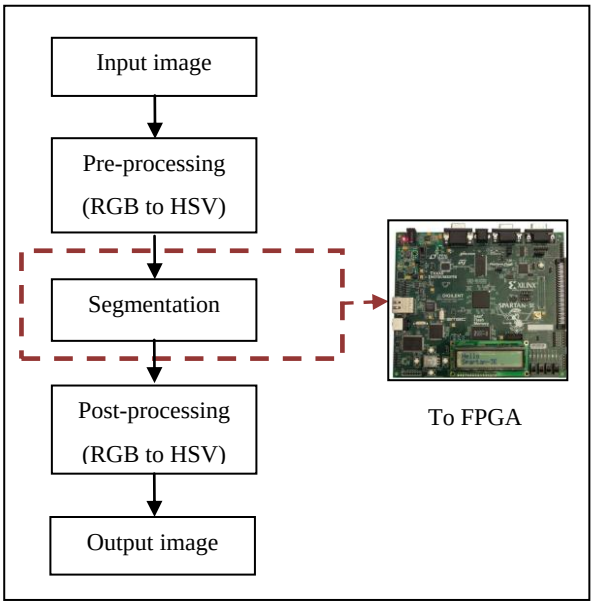

Fig. 1. Block diagram of ALL segmentation

The pre-processing and post-processing steps for ALL segmentation are proposed using Simulink blocks. Fig. 2 presents color space conversion block from RGB to HSV image and applying median filter to H channel for further processing.

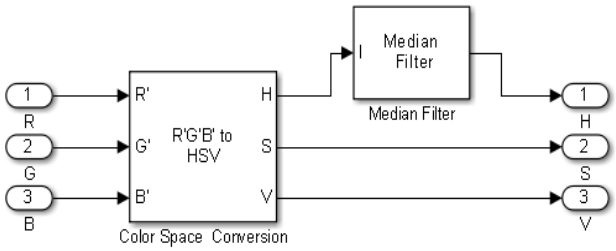

Fig. 2. Pre-processing for ALL segmentation

III. Proposed Framework

A. Hardware Design

To accomplishing Image processing task using Xilinx System Generator, two Software tools are needed to be installed. This work uses MATLAB version R2012b and Xilinx ISE 14.5. The model is built for image segmentation using library provided by Xilinx Blockset. According to the design of segmentation to meet hardware requirements, pre-processing the HSV image prior to the main hardware architecture is needed due to the nature of hardware that deals with an image as a vector. Also, image post-processing is required. There are three stages involved in ALL hardware segmentation process using Simulink and Xilinx blocks:

- Hardware pre-processing
- Xilinx models for HW segmentation
- Hardware post-processing

Fig. 3 represents the main block diagram of proposed framework.

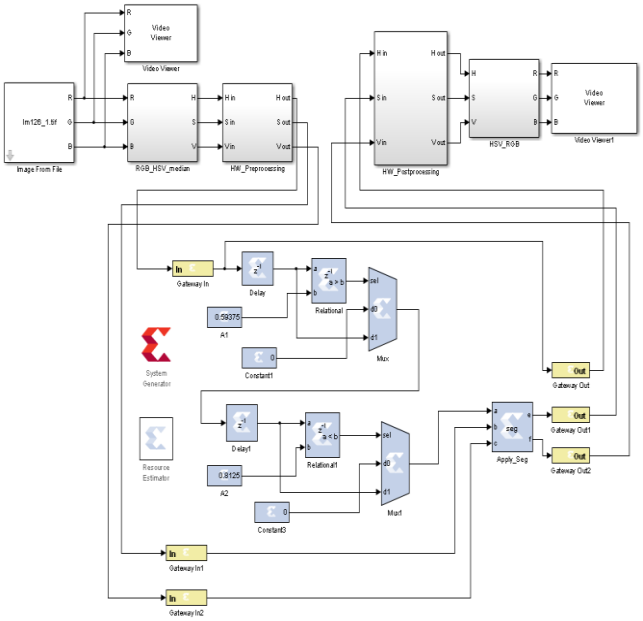

Fig. 3. Block diagram of proposed framework

The image pixels are provided to Xilinx models in the form of multidimensional H|S|V separate color signals in the form of vector in Xilinx fixed point format. The reflected results can be seen on a video viewer. Once the expected results are obtained, XSG is configured to be suitable for SPARTAN-3E XC3S500E-FG320.

a) Hardware Pre-Processing

Pre-processing blocks provide an input image suitable for FPGA as vector array. Reshape blocks convert the HSV image channels into single array of pixels. The process of setting sampling mode is obtained using frame conversion. Unbuffer blocks convert this frame to scalar samples output at a higher sampling rate. The model based design used for image pre-processing for FPGA is shown in Fig. 4.

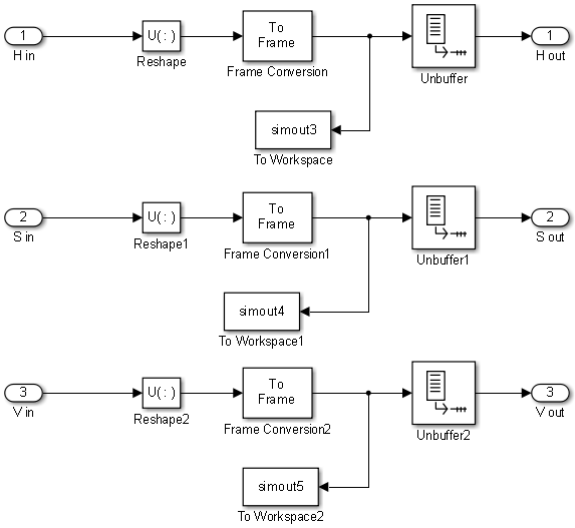

Fig. 4. Hardware Pre-processing

b) Xilinx Models for HW Segmentation

Hardware segmentation process is modeled using Xilinx blocks. Once the FPGA boundaries have been established using the Gateway In and Gateway Out blocks, the DSP design can be constructed using Xilinx DSP blocks. Within the Gateway In and Gateway Out blocks, Simulink blocks are not supported for use.

Xilinx fixed point type conversion is made by Gateway In blocks. Image Segmentation process is achieved based on two angle values that obtained from color histogram of H channel. These two values are represented using two constant blocks. Multilevel thersholding operated using Relational and Mux blocks. This is followed by certain blocks to merge all the processed data. Fig. 5 shows the ALL segmentation using Xilinx blocks.

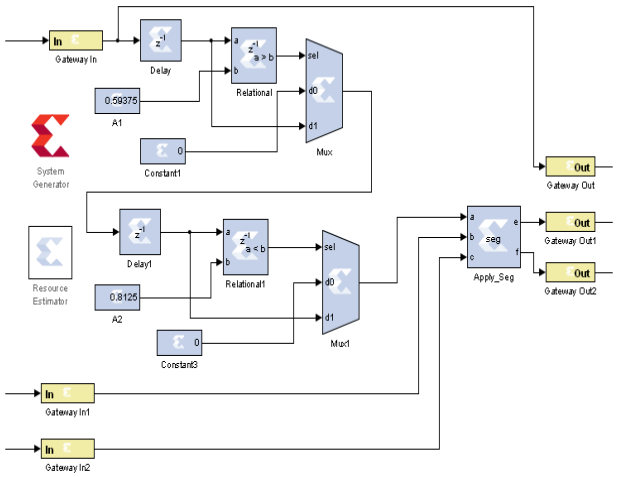

Fig. 5. ALL Image Segmentation Using Xilinx blocks

c) Hardware Post-Processing

Post-processing blocks converts an image from vector to 2D matrix as shown in fig. 6. Buffer blocks are used to convert scalar samples to frame output at lower sampling rate. The process of converting 1D image to 2D image is obtained using reshape blocks.

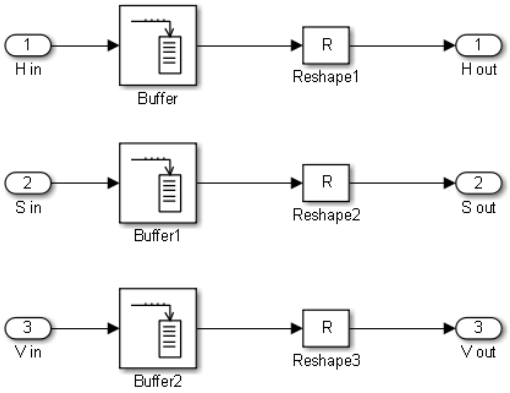

Fig. 6. Hardware Post processing

B. Hardware Co-Simulation

Once the results are obtained from hardware design; the model is implemented for JTAG hardware co-simulation. The System generator parameters are set and generated. On compilation, programming file in VHDL is created to be accessed by Xilinx ISE. The module is synthesized and implemented on FPGA. Fig. 7 illustrates the hardware co-simulation block.

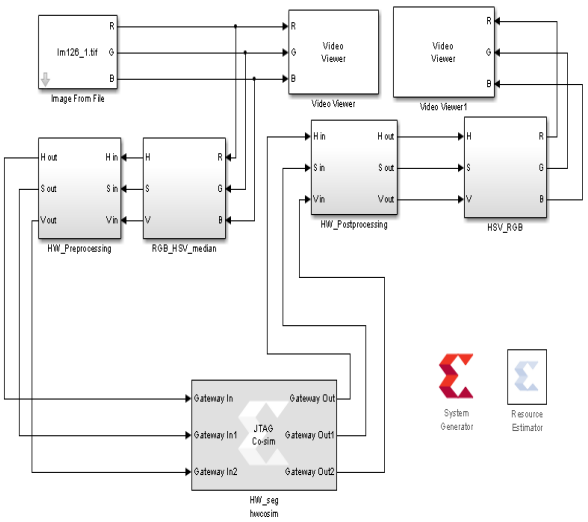

Fig. 7. Hardware co-simulation

Fig. 8 presents the RTL schematic of the resulting circuit for hardware segmentation.

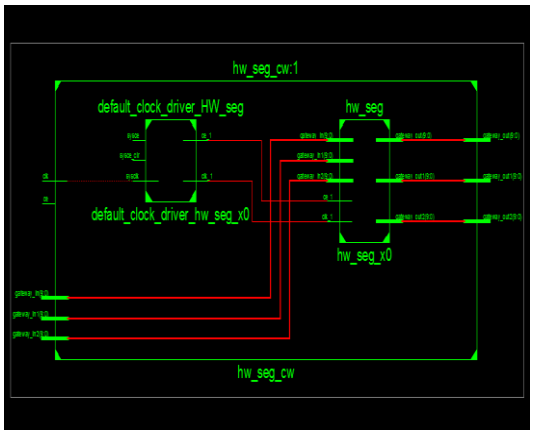

Fig. 8. RTL Schematic for Hardware Segmentation

IV. Results and Discussions

Microscope Images of ALL are taken from ALL-IDB database [20]. The images of the database have resolution 256 × 256. Figure 9 shows the sample of ALL images.

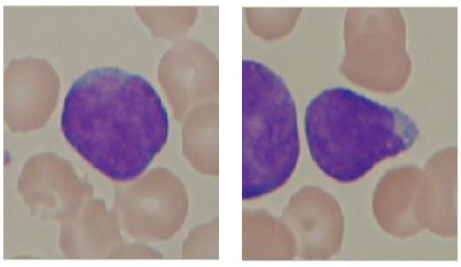

Fig. 9. Sample of ALL images

The SPARTAN-3E (XC3S500E-FG320) resource usage is estimated for proposed framework as shown in table 1. The VHDL code for the proposed hardware segmentation has 2381 lines of VHDL code. This is due to the huge amount of floating point-fixed point conversions.

TABLE I. Device Utilization Summary

Resource	Used	Available	Utilization
Flip Flop	22	9312	1%
Slices	30	4656	1%
LUTs	39	9312	1%
IOBs	61	232	26%
Minimum period: 3.524ns (Maximum Frequency: 283.768MHz) Minimum input arrival time before clock: 1.973ns Maximum output required time after clock: 8.766ns Maximum combinational path delay: 6.113ns			

The original image of ALL is shown in Fig. 10 while the resulted image after hardware segmentation is represented in fig. 11.

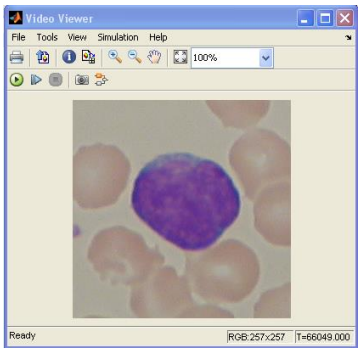

Fig. 10. Original ALL image

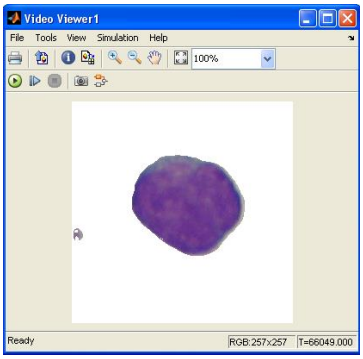

Fig. 11. Resulted ALL image

V. Conclusion

In this work, the hardware segmentation framework based color histogram of Hue channel of HSV color space is proposed. The results obtained from the Xilinx and Simulink model showed that the proposed framework achieved a superior performance and quality. In term of the device utilization, the implementation occupies around 1% of the used SPARTAN-3E XC3S500E-FG320 FPGA. In the proposed framework, the interfacing of Matlab and XSG is done. The ALL Image segmentation is performed on Matlab as well as Simulink Model and it has been verified using SPARTAN-3E XC3S500E-FG320 FPGA.

In the future work, the design framework used in this work will be optimized and implemented on other Xilinx FPGA Kits such as Virtex-7.

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