CPLD-Based Circuit Design of IGBT Dead-Time Compensation

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***Abstract*—IGBT (insulated-gate bipolar transistors) dead-time compensation circuit has a very important significant for improving the output voltage waveform of the inverter, reducing the harmonic output current. Thus, many compensation strategies are reported in literatures and have been implemented in industrial drives recently. Overall, the method of dead-time compensation can be divided into hardware compensation and software compensation. Hardware compensation method needs additional hardware circuits, which means additional space and cost. Still more, the additional circuit is easy to interfere with others, which can reduce the compensation accuracy. While the software compensation method takes up a lot of memory space and additional input-output ports of processor, which often result to the added operation and heat dissipation of controller. In this paper, CPLD (complex programmable logic device)-based circuit design of dead-time compensation is presented to solve these existed drawbacks. It is verified that not only can the circuit simplify existed inverter dead-time compensation design, but also it has the advantages of small volume, strong anti-interference ability, and high compensation precision. The simulation results validate that this method is feasible and effective.**

***Keywords*—Dead-time compensation; inverter; compensation method; circuit design; CPLD; IGBT**

I. INTRODUCTION

Power electronic devices are not ideal, which its action has a finite turn-on and turn-off time. People join in the time delay, called dead-time control, of the gate drive in order to avoid the shoot-through of inverter arms. Dead time is consist of power switching dead time and dead-time control and effects caused by dead time called the dead-time effect of the inverter. The existence of dead-time effects has a great influence on the inverter. When the dead time is longer, the inverter output fundamental voltage loss will become greater and the voltage waveform distortion is more severe; when the magnitude of the load current is decreased, the current waveform distortion will more serious. The dead-time effects not only affect the amplitude of the output voltage, but also have an impact on its phase. However, the PWM waveform is no longer symmetrical to the center, so that the magnitude of the space voltage vector will produce deviations and phase also change. In view of this, the impact of the dead time more and more caused people's attention; the dead-time compensation has become particularly important. Therefore, the domestic and foreign scholars carried out a lot of work to study and explore the problem of converter dead-time compensation.

Various compensation strategies have been proposed [1]–[16] to overcome the negative effect of dead time. The current research on the inverter dead-time compensation focused on the voltage feed-forward and current feedback compensation. Through the error analysis between the inverter reference voltage and the output voltage, paper [2] proposes a simple and feasible compensation method based on the dead time and the DC bus voltage; but due to lack of compensation for the power devices turn-on voltage drop, so there is the existence of compensation error. The inverter snubber and parasitic capacitance are considered when doing dead-time compensation in paper [3]. Based permanent magnet synchronous motor (PMSM) AC servo system, papers [6]-[7] use disturbance observer approach to achieve inverter dead-time compensation online for the dead time effect; the rotor d-q axis voltage caused by the non-ideal characteristic of the switching device and inverter dead time is regarded as the disturbance voltage to estimate online and then feedback to the inverter reference voltage to carry out feed-forward compensation. Because of the setting of disturbance observer, the method exist phase lag for compensation voltage, while the transmission gain selection of disturbance observer requires some experience. Paper [8] adopt a zero voltage vector splitting method to solve the zero current clamp problem caused by inverter dead time, however the dead time impact for voltage still need to compensate. Paper [13] takes into account the voltage compensation and elimination of zero current clamp effect, but because of correlation between the compensation voltage and the operating point, the zero current clamp phenomenon still exist compensation error. Summers T. et al [14] reduce the problem of zero current clamp used the predictive current control, but the systems is a local stability.

Currently, methods of achieving inverter IGBT dead-time compensation mainly exist two categories: the hardware

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compensation and software compensation. Hardware compensation is needed to provide additional hardware circuit, and need to compare the actual voltage and voltage reference value, and then get the desired compensation voltage signal , so it is necessary to take up more hardware resources , each part of the circuit also generate interaction, causing the compensation precision is reduced. Software compensation need to add the dead-time compensation algorithm in the motor drive control program to achieve compensation for the dead zone, this method requires a large amount of memory resources occupied control chip, increasing the control processor's burden, affecting the running speed and the heat dissipation effect. These designs, CPLD dead-time compensation logic circuit, verify the feasibility and effectiveness through simulation tests in Modelsim.

Therefore, the power electronics technology need for a good inverter dead-time compensation circuit, it takes up a less hardware resources occupied various parts of the circuit and do not affect each other, the control chip run faster and excellent heat dissipation. This design uses the CPLD chip replace complex hardware circuit, using HDL (Hardware Description Language) to generate its internal logic circuit instead of software compensation algorithms, realizing inverter IGBT dead-time compensation. These designs, CPLD dead-time compensation logic circuit, verify the feasibility and effectiveness through simulation tests in Modelsim.

II. Internal Structure and Description of the CPLD

With the development of electronic technology and the continuous improvement of ASIC technology, the design of digital system is moving fast, large capacity, small volume, light weight in this direction. However, CPLD (Complex Programmable Logic Device) has been widely used in the design of electronic circuits and system because of its flexibility, modifiability, and short development cycle. Substitute for the traditional electronic circuit has incomparable advantages:

1)high integration, small discrete components, high anti-interference ability; 2)simple circuit design is and convenient, software design, easily modified; 3)Ease of product upgrading; 4) the use of high frequency oscillator, easy high speed processor (e.g. DSP) connection, high frequency control system. Based on this, the author uses ALTERA series MAX II CPLD to produce SPWM wave for IGBT bridge driver. The design operation is stable, strong anti-interference, safe and reliable.

The following describes the hardware configuration of the whole design.

The hardware structure in this design is mainly composed of the serial port module, dead-time compensation module, dead-time insertion module, protection module and output control module, as shown in Fig. 1.

The controller calculates the switching time of six IGBT switches and sent CPLD chip the messages via 6 data bus. The internal logic circuits of CPLD firstly compensate dynamic dead-time and then insert the dead-time. According to the control requirements, serial port module decides whether to compensate for the switching time.

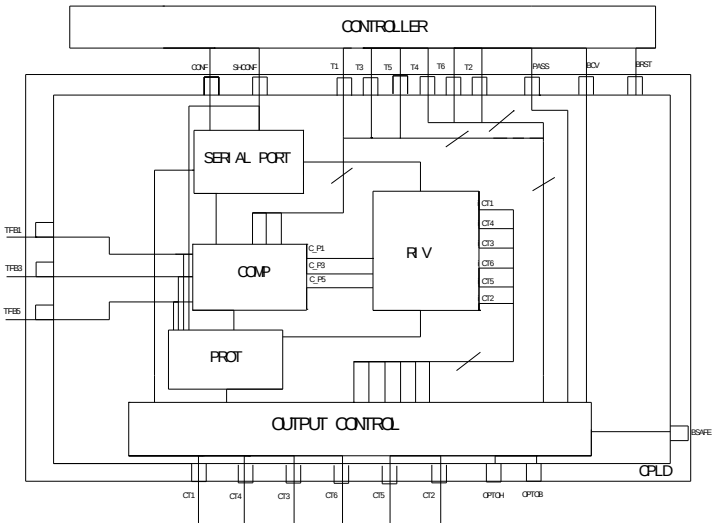

Fig. 1. CPLD internal structure

If it claims for compensation, the dead-time compensation module calculates the real-time dynamic compensation time to insert the dead-time. During the whole process, a real-time protection function can be done by protection module, such as the over-current, over-voltage and open circuit, etc.

III. Program Realization

Verilog HDL and VHDL are currently most popular hardware description language (HDL: Hardware Description Language) in the world, are the IEEE standard and have been widely used in the project development based on programmable logic devices. Both are developed in the mid-1980s, the former by Gateway Design Automation, Inc. (acquired by Cadence in 1989) and the latter by the US military.

In text form to describe the hardware structure and behavior of digital systems, HDL is a language with a formal way to describe digital circuits and systems and describe their design ideas from the upper to the lower layer. In other words, it uses a series of sub-level modules to represent complex digital systems to verify the simulation layer by layer, and then the specific combination of modules converted into a gate-level netlist by the synthesis tool that put into a specific circuit structure by the layout tools. At present, this top-down approach has been widely used. Generally speaking, HDL contains the following main features:

- HDL structure contains some form of high-level programming language and also take into account the specific structure described the hardware circuit connection.
- HDL can describe the design at different abstract levels through the use of structural level behavioral description. It is a top-down digital circuit design method, including three areas and five abstract levels.
- HDL is processed in parallel and has the ability to perform multiple tasks at one time. This feature is

different from the general advanced design languages (such as C language, etc.) which use serial execution.

- HDL has a concept of timing. General, advanced programming language is no concept of timing, but the hardware circuit is always a time delay from input to output, it needs to introduce the concept of time delay in order to describe this feature. HDL can not only describe the function of the hardware circuit, but also describe the timing circuit.

In this design, using HDL writes programs to achieve CPLD internal function of each module.

A. Dead-time compensation

In order to make the compensation more accurate and effective, this bloc consider the time of both the transition from ON to OFF and effect of inverter snubber. The following introduced the proposed compensation method. These functions restore the time value pulses on the IGBT gates for matching the theoretical commands, after all distortions of them (due to dead time and distortion trough the command channel).Timing diagram is shown in Fig. 2.

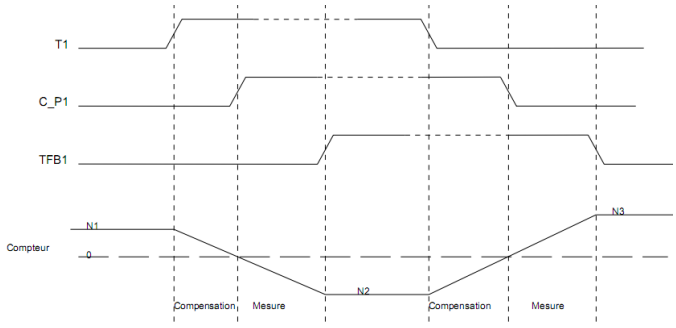

Fig. 2. Dead-time compensation timing diagram

At the rising edge of T1, the counter is at N1 value, this is the value to compensate, the counter is counting down till it reaches zero, at this time C_P1 is rising as the new theoretical command to apply, and the counter is still counting down till the rising edge of TFB1 which is the real application of the voltage on the phase. The time difference between C_P1 and TFB1 is due to the dead time and also the delay of all the components. At this time the counter is in stand-by, and it has N2 value which is the error to compensate (to add) at the next edge.

At the falling edge of T1, the counter is counting up from the N2 value till it reaches zero, at this time C_P1 is falling as the new theoretical command to apply, and the counter is still counting up till the falling edge of TFB1 which is the real application of the voltage on the phase. Now, the counter has N3 value which will be compensated at the next rising edge of T1, as explained with N1.

For example, the frequency of the clock signal is f and dead timer is n bits, then the compensation resolution is 1/f and the maximum compensation value is $2^n * (1/f)$. For this design, f=40 MHz, n=10, the maximum compensation value is 25us and the compensation resolution is 25ns. Flow chart is shown in Fig. 3.

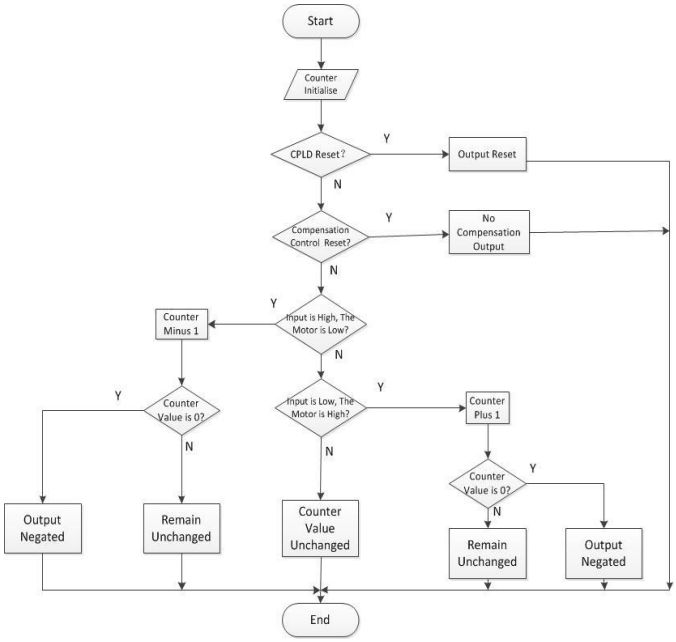

Fig. 3. Dead-time calculation flow chart

B. Dead-time insertion

This bloc adds the dead time at the compensated pulses, and drives directly the 6 outputs for transistors commands. Timing diagram is shown in Fig. 4.

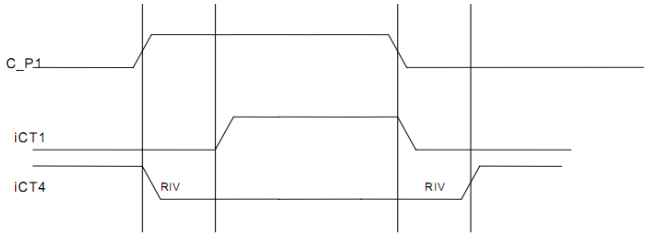

Fig. 4. Dead-time insertion timing diagram

For the same bridge arm of switch tube, at the rising edge of C_P1, iCT4 is falling, iCT1 is rising after the dead time INSE; at the falling edge of C_P1, iCT1 is falling, iCT4 is rising after the dead time INSE. It is the same rule for the others branches. Flow chart is shown in Fig. 5.

C. Serial port

A serial port offers the controller the capability to configure the CPLD by writing into the REGCONF register. SHCONF is used to shift signal for REGCONF register. CONF is data serial input and the configuration bits are applied to the MSB of the REGCONF register.

After RESET, the CPLD is in a configuration mode, the controller is able to write the configuration into the REGCONF register. In this mode the outputs CT1… CT6 are not driven. For getting out of this mode, the controller applies a falling edge on the BCV, and the CPLD goes in a normal mode, the REGCONF register is locked. But as soon as the circuit is in normal mode, the T1, T3, T5 inputs are interpreted and the outputs CTi can commute. Timing specifications are shown in Table 1.

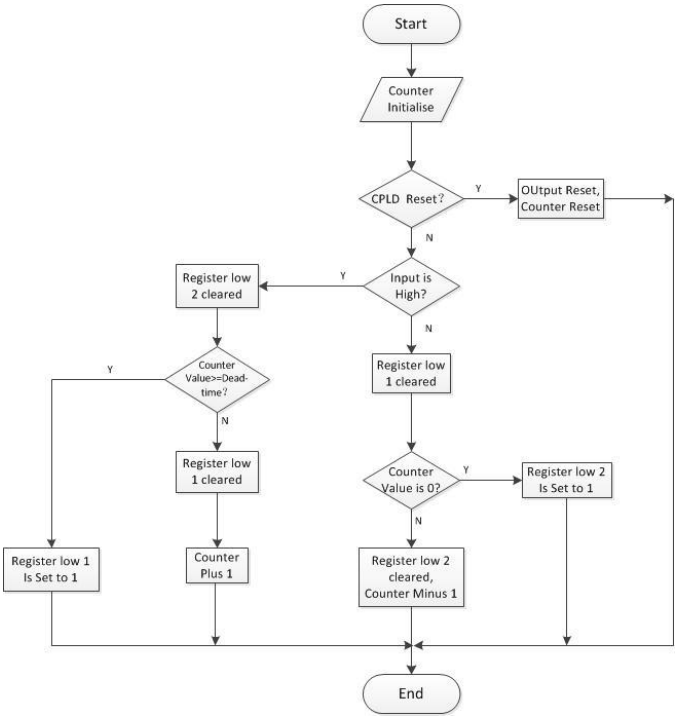

Fig. 5. Dead-time insertion flow chart

TABLE I. TIMING SPECIFICATIONS

Symbol	Description	Min	Unit
Ton	Time for SHCONF at level High	100	ns
Toff	Time for SHCONF at level Low	100	ns
Ts	Setup time for CONF on rising edge of SHCONF	0	ns
Th	Setup time for CONF on falling edge of SHCONF	0	ns

D. Output control

According to the states of the circuit, this Bloc applies the orders on Outputs CTi. In PASS state, all defaults detections are still activated. The Outputs CT1 …CT6 can drive up to 24mA. As shown in Table 2.

TABLE II. STATES OF CIRCUIT

States	Conditions	Outputs CT1…CT6
Reset	BRST=0	0 0 0 0 0 0
PASS	PASS=1	0 0 0 0 0 0
BSAFE	BSAFE=0	0 0 0 0 0 0
Normal	BCV=0	iCT1…iCT6
CONFIGURATION	Until falling edge of BCV	0 0 0 0 0 0

IV. SIMULATION RESULTS

A. Theoretical waveforms

This paper is the inverter IGBT dead-time compensation circuit design based on CPLD. According to the description of each module and the port function, we can draw the waveform of this design theory. Theoretical waveforms are shown in Fig. 6.

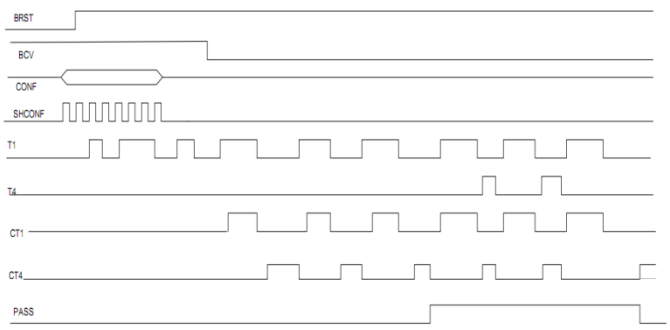

Fig. 6. Theoretical waveforms

B. Simulation waveforms

For the dead-time compensation method simulated test in Modelsim simulation platform. In the simulation of just one phase of bridge arm simulation, given the incentive program to simulate the actual circuit can be obtained by simulation results, the simulation waveform as shown in Fig. 7.

From the simulation waveform can be seen, at the falling edge of BCV, serial port module activates output control module, CT1 and CT4 are the output signal through an output port; the serial port module, dead-time compensation module, dead-time insertion module, protection module is not activated. Control output signal output control module for repeating the input signal. Output control module of control output signal ensures that the output signal is the input signal. At the rising edge of PASS, this function of dead-time compensation is inhibited.

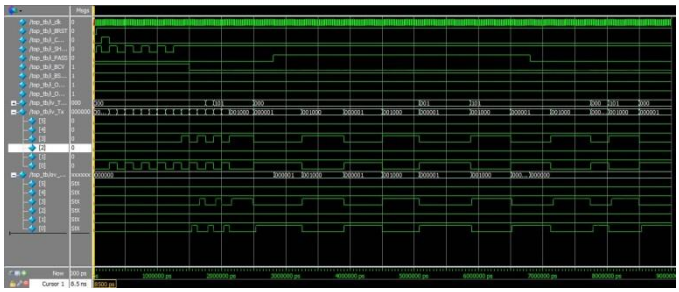

Fig. 7. Simulation waveforms

V. CONCLUSION

This paper mainly studies the problem of inverter IGBT dead-time compensation, proposed the dead-time compensation circuit design based on CPLD. First of all, starting from the hardware circuit describes the internal structure and function. Secondly, the software realization details programming ideas and flow chart.

Compared with the previous design, we can see that

- The design of the serial port module, dead-time compensation module, dead time insertion module, protection module and output control module is focused on a CPLD chip. Compared with the hardware compensation, each circuit section does not influence each other; the design takes less hardware resources and has the advantages of strong anti-interference ability, high compensation precision.

- Compared with the software compensation ,the motor control without adding driver dead-time compensation algorithm save control chip memory resources and the control chip run faster and excellent heat dissipation , and thus switch of the same bridge arm never occurs simultaneous conduction since switching speed , meanwhile have high compensation accuracy.

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