Real-Time Implementation of an Open-Circuit Dc-Bus Capacitor Fault Diagnosis Method for a Three-Level NPC Rectifier

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***Abstract*—The main goal of this paper is to detect the open-circuit fault of the electrolytic capacitors usually used in the dc-bus of a three phase/level NPC active rectifier. This phenomenon causes unavoidable overvoltage across the dc-bus leading therefore to the destruction of the converter's power semiconductors. The real-time detection of this fault is therefore vital to avoid severe damage as well as wasted repair time. The proposed diagnosis method is based on the measurement of the voltages across the two dc-bus capacitors. Their mean values are therefore compared with the half value of the dc-bus reference voltage. If the comparison result is under a predefined threshold value, a fault alarm signal is generated in real-time by the monitoring system. The converter's control algorithm and fault detection method are both implemented in real-time on a DSP controller. The obtained experimental results confirm the effectiveness of the proposed diagnosis technique. Indeed, a fault signal is generated at the peripheral of the DSP after 60 ms of the fault occurrence.**

***Keywords*—fault detection; capacitor failure; open-circuit fault; real-time implementation; multilevel converters**

I. INTRODUCTION

Multilevel converters are without a doubt the best suited topologies for medium voltage/ medium power industrial applications [1]. They have many attractive advantages as compared with two-level converters such as reduced dV/dt, lower voltage stress across power semiconductors, better quality of the output voltages, reduced filter size, etc. [2,3]. Among several power conversion structures, the three-phase three-level Neutral Point Clamped (NPC) is widely preferred since it needs only one dc source and the minimum number of dc-bus electrolytic capacitors.

As any power conversion device, the electrolytic capacitors used in the dc-bus, the power transistors and diodes are the most vulnerable power components of the NPC converter. Usually, the resulting faults remain a serious trouble to be identified in order to avoid significant damage of the remaining converter's components and circuits [4].

Many diagnosis methods have been proposed in the recent literature to identify the open-circuit fault of power transistors and diodes utilized in the three-level NPC converter [5,6,7,8,9,10]. Some of the diagnosis and faulty components identification methods are based on the analysis of the instantaneous pole voltage and its duration [5], as well as the currents in the dc-bus neutral point. The latters (pole voltages and current in the mid-point) are compared with their estimated values which are computed in terms of the switching states and dc-bus voltage or phase currents. Some other methods are based on the analysis of the average current Park's vector [7], the normalized average current [8], the phase current distortion [9], the slope method [10], etc.

The diagnosis of the dc-bus capacitor failures for NPC converters has not been addressed until now. The research works on this issue are restricted right now to the case of three-phase two-level PWM converters, DC-DC converters, and diode rectifiers. In [11], an on-line estimation of the internal Equivalent Series Resistance (ESR) of the dc-bus electrolytic capacitor of a three-phase two-level AC/DC converter was proposed. The method is based on the injection of a ripple term in the phase currents and the analysis of its effect on the dc-bus voltage waveform. The least square algorithm is used to estimate the ESR value of the capacitor. However, this method can be utilized only when the converter is controlled with the space vector modulation scheme (SVPWM). In [12], a capacitor failure detection method was proposed for a three-phase diode rectifier. The method is based on the analysis of the 6^{th} harmonic component of the dc-bus voltage to detect the capacitor aging and open-circuit faults. Though this method is very simple, but it requires the knowledge of the load and supply conditions.

This paper is focused on the diagnosis of open-circuit faults of the dc-bus capacitors in three phase/level NPC converter operating as an active ac/dc rectifier. The detection method is performed by means of the measurement of the average value of the voltage across the upper and the lower dc-bus capacitors. If the comparison result exceeds a predefined threshold value, a fault alarm is generated in real-time. In this manner, harmful effects on other components are avoided and maintenance rescue can be done in safety. Notice that, no additional devices or sensors are needed to implement this method.

The manuscript is organized as follows: Section II presents the three phase/level NPC active rectifier operation principle with a brief description of its electric circuit as well as its current control algorithm. The effect of the open-circuit fault of a dc-bus capacitor on the performance of the converter and the proposed diagnosis method are explained in section III. Experimental results are given in section IV to evaluate the

performance of the proposed fault detection method. Finally, the work is concluded in section V.

II. Operation of Three Phase/ Level NPC Rectifier

A. NPC topology

The three phase/level NPC converter shown in Fig. 1 consists of three legs (k = 1, 2, 3). Each leg is built using four-quadrant switching devices labeled $T_{ki\ (i\ =1,..,4)}$, and two clamping diodes $D_{kj\ (j\ =1,..,6)}$. Moreover, the dc-bus is made with two capacitors connected in series: C_{dc}^{up} is the upper capacitor connected to the dc-bus positive rail; C_{dc}^{low} is the lower capacitor connected to the negative rail. The point of common connection is named midpoint "O". Basically, the two capacitors C_{dc}^{up} and C_{dc}^{low} should have the same value C_{dc}. Accordingly, the voltage across each capacitor is given as follows:

$$\begin{cases} V_{po} = \dfrac{1}{C_{dc}} \int i_c^+ dt + \dfrac{V_{dc}}{2} \\ V_{on} = -\dfrac{1}{C_{dc}} \int i_c^- dt + \dfrac{V_{dc}}{2} \end{cases} \quad (1)$$

For each leg there exist three possible switching states of the power semiconductors designated by "P", "O", and "N". The corresponding pole voltage referred to the midpoint "O" can therefore take three levels: $+V_{dc}/2$, 0, and $-V_{dc}/2$. More details on the operation principle of this power conversion topology can be found in [13].

B. Operation principle as an active rectifier and control algorithm

As illustrated in Fig. 1, in this operation mode, the ac terminals of the converter are connected to the grid voltages through three inductors which operate as low-pass filter to eliminate the high frequency components of the line currents. The dc terminals are connected either to a passive load that consumes the active power or to an active load that provides the active power such as photovoltaic generator or wind turbine [14].

When this converter operates as an active rectifier, two objectives need to be achieved. First, it should regulate the voltage across the dc-bus according to a target reference. Second, it should generate a high quality of the line currents with a perfect control of the reactive power exchanged with the grid. The latter needs to be equal to zero so as to achieve unity input power factor operation. In the upper part of Fig. 1, we illustrate a simplified schematic block diagram of a conventional Voltage Oriented Control (VOC) algorithm that is used to achieve the aforementioned performance. First a PI controller compares the target reference (V_{dc}^{ref}) and the measured value of the dc-bus voltage and computes the reference of the d-axis component of the line current (i_d^{ref}). As for the reference for the q-axis component of the same current (i_q^{ref}), it is set to zero.

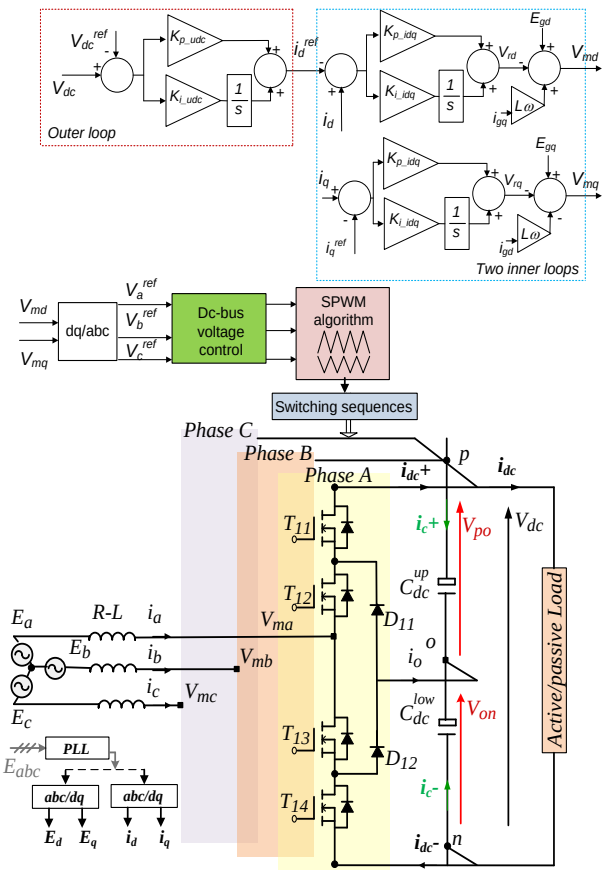

Fig. 1. Grid connected NPC rectifier with its VOC control algorithm

Two additional PI controllers are therefore used to compare i_d^{ref} and i_q^{ref} with the d-q axis components of the measured line currents. The obtained control-laws V_{md} and V_{mq} are transformed into the three-phase reference frame to obtain the suitable modulation signals namely V_a^{ref}, V_b^{ref}, and V_c^{ref}. Finally, the conventional multicarrier PWM algorithm is utilized to generate the appropriate gates pulses of the power transistors.

III. Open-Circuit Fault of the Dc-Bus Capacitor

Basically, the electrolytic capacitors failures are classified into two types [12]. 1) Capacitor aging due to the evaporation of the electrolyte liquid. This phenomenon leads to the increase of the internal Equivalent Series Resistance (ESR) and the decrease of the capacitance as well. 2) The open-circuit fault due to the sudden disconnection of one or more capacitors from the dc-bus. This phenomenon may be due to PCB or connector failures. As a consequence of this abrupt change, a sever overvoltage due to the commutation process of the power semiconductors appears across the dc-bus. Moreover, and inherent unbalance arises between the two voltages V_{po} and V_{on}.

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A. *Diagnosis of the open-circuit fault effect on the converter's performance*

To evaluate the effect of open-circuit fault of one dc-bus capacitor on the performance of the NPC rectifier, computer simulations are carried out using a numerical model of the converter. The du-bus voltage reference is set to 100 V. the maximum amplitude of the line-to-line grid voltages is equal to 50 V. The remaining parameters of the power conversion circuit and controllers' gains are reported in Table I. An abrupt open-circuit fault of C_{dc}^{up} was programmed to occur at time t = 1.5 s (Fig. 2). Fig. 3 displays the waveforms of V_{po}, V_{on} and the midpoint voltage $V_o = V_{po} - V_{on}$. One can observe that V_{po} decreases abruptly to zero, after that, its waveform becomes distorted with a chattering phenomenon leading to an overvoltage across the capacitor C_{dc}^{up}. This overvoltage may lead to the destruction of the remaining power semi-conductors. In practice, the measurement and computation of the average value of V_{po} is not easy to accomplish due to the high frequency chattering. As for V_{no}, its amplitude bends down slowly without any distortion or chattering. Therefore, it can be concluded that this voltage contains useful information on the state of health of C_{dc}^{up}. On the other hand, one can also observe that the voltage V_o is affected by this fault where a high frequency fluctuation occurs around the zero voltage value. Fig. 4 illustrates the waveforms of the line currents i_a, i_b, and i_c. One can observe that the waveforms are quite sinusoidal and balanced before the fault. However, their amplitude decreases suddenly after the fault; low-order harmonic components appear also in the line currents waveforms. Therefore, it can be concluded, that this phenomenon causes a substantial decrease of the active power being transferred to the load as well as a distortion of its waveform. Fig. 5-a shows that the phase a line current is in phase with its corresponding grid voltage E_a. However, after the fault, the converter loses its performance of producing a line current in phase with the grid voltage. Fig. 5.b displays the waveform of the q-axis component of the line current. Before the fault, this current is quite equal to zero which means that zero reactive power is exchanged with the grid. However, after the fault, the q-axis current oscillates at low frequency near the zero value. Therefore, the reactive power remains near zero; however its waveform will include low frequency distortions.

TABLE I. EXPERIMENTAL SETUP'S PARAMETERS

Parameters	*labels*	*Values*
Grid frequency	$F_{central}$ (Hz)	50
Switching frequency	f_{sw}(kHz)	3.33
DC bus capacitor	C_{dc} (F)	940e-6
Input filter inductance	L (H)	10e-3
Filter resistor	R (Ω)	1
R-Load	Rload (Ω)	150
Cascaded linear PI controller		
Proportional gain of PI linear parameter of voltage loop V_{dc}	K_p^{Vdc}	5
Integral gain of PI linear parameter of voltage loop V_{dc}	K_i^{Vdc}	10
Proportional gain of PI linear parameter of current controller	K_p^{I}	10
Integral gain of PI linear parameter of current controller	K_i^{I}	250

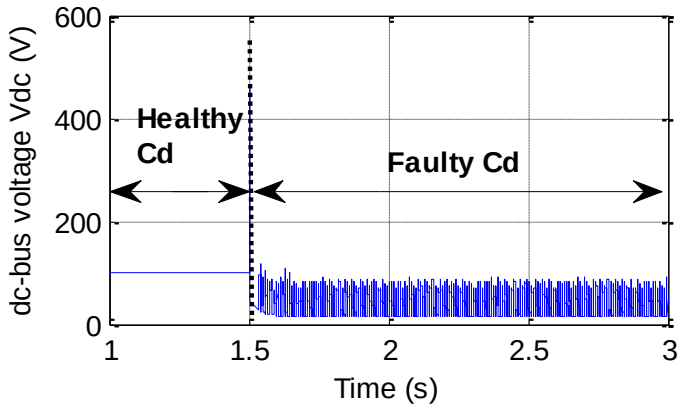

Fig. 2. Dc-bus voltage (Vdc) waveform under healthy and open-circuit faulty conditions (an open-circuit fault of C_{dc}^{up} is triggered at time t =1.5 s)

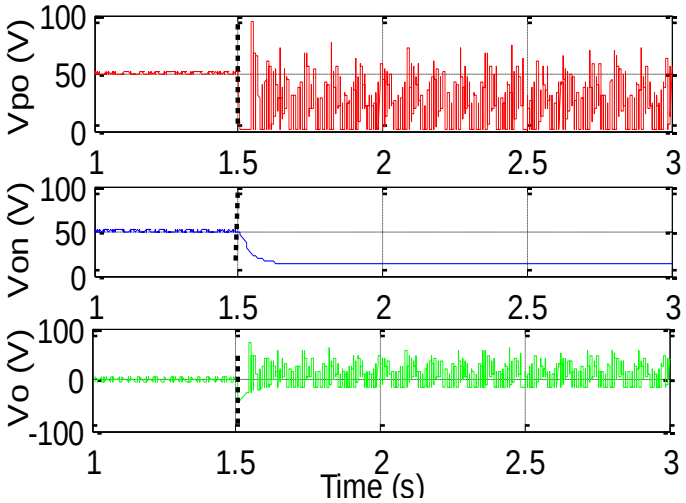

Fig. 3. From top to bottom: Voltages Vpo, Von, and Vo under healthy and open-circuit faulty conditions (an open-circuit fault of C_{dc}^{up} is triggered at time t =1.5 s)

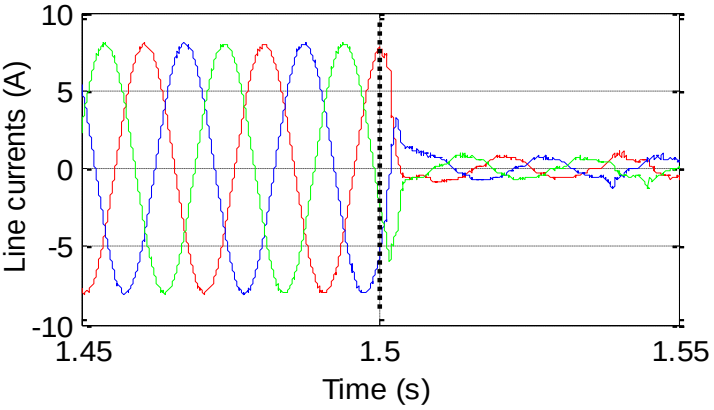

Fig. 4. Line currents waveforms under healthy and open-circuit faulty conditions (fault occurred at t = 1.5 s)

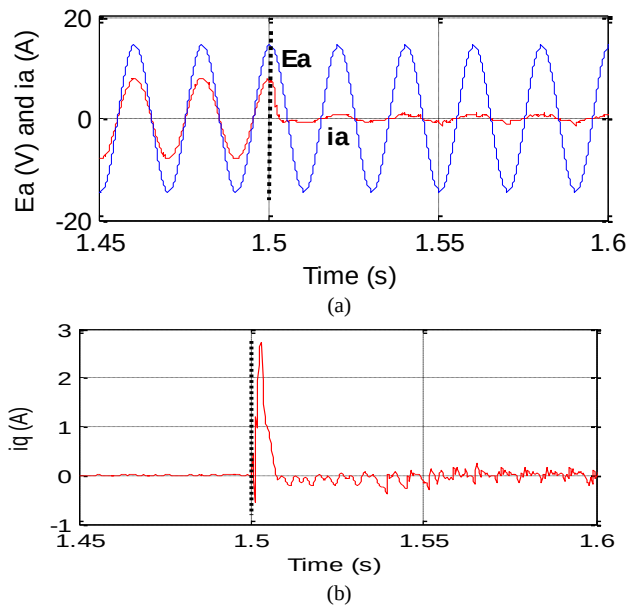

Fig. 5. (a) Line current i_a and line voltage E_a, (b) reactive current i_q under healthy and faulty conditions

B. Capacitor open-circuit fault detection method

Occurrence of open-circuit fault can be diagnosed by monitoring the two dc-bus voltages V_{po} and V_{on}. At each sampling period, these voltages are measured using the same voltage sensors installed with the converter to perform the control algorithm of the rectifier. After that, the average values V_{po}^{Av} and V_{on}^{Av} are computed and compared to the half value of V_{dc}^{ref}. The three following states can therefore occur:

- If $\frac{V_{po}^{Av}}{V_{dc}^{ref}/2} \leq$ predefined threshod value , therefore an open-circuit fault affected the lower capacitor C_{dc}^{low}
- If $\frac{V_{on}^{Av}}{V_{dc}^{ref}/2} \leq$ predefined threshod value , therefore an open-circuit fault affected the upper capacitor C_{dc}^{up}
- Else, both capacitors are healthy.

Fig. 6 displays the flowchart of the proposed diagnosis method.

IV. Experimental Validation based on Real-Time Diagnosis

In order to testify the effectiveness of the proposed open-circuit fault detection method, the VOC algorithm of the NPC rectifier, and the diagnosis algorithm are implemented in real-time on the DSP TMS 320F28335 of Texas Instruments running at a clock frequency of 150 kHz. Both algorithms are edited using Simulink software. The code is thereafter compiled using the real-time workshop of Matlab and Code Composer Studio (CSS). On the other hand, a laboratory prototype of the NPC converter was built using the power transistors IRF460 and the clamping diodes 15ETH06. A twelve-bit analog to digital converter (ADC) with a conversion rate of 80 ns is used for data acquisition. The open-circuit fault is emulated using a solid state relay that is connected in series with the upper dc-bus capacitor C_{dc}^{up}. Fig. 7 illustrates a photo of the experimental setup. The remaining parameters of the experimental setup and controller are quite similar to those used in simulation.

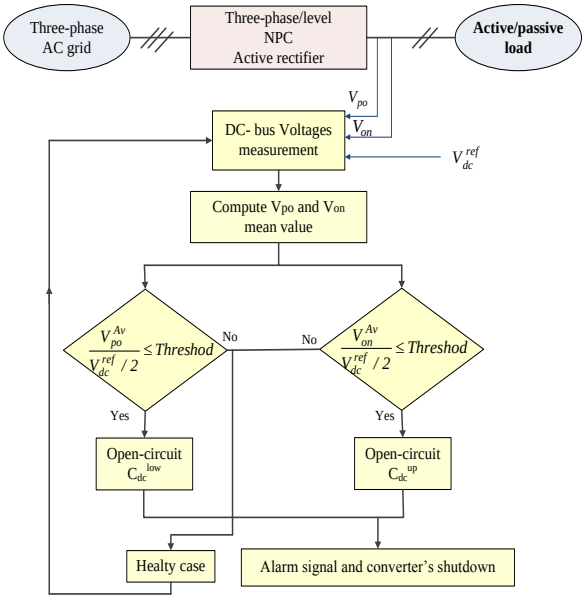

Fig. 6. Flowchart of the proposed dc-bus capacitor fault detection

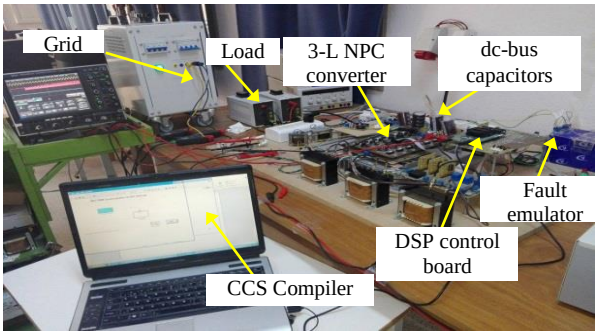

Fig. 7. Experimental setup of a three phase/level NPC active rectifier with faulty dc-bus capacitor

Fig. 8 shows the experimental results obtained under healthy condition and also under an open-circuit fault of C_{dc}^{up}. It is clear that the waveforms of the line current i_a, dc-bus capacitor voltages across C_{dc}^{up} and C_{dc}^{low} , and the voltage V_o are quite similar to those obtained with computer simulations which validates the analysis done in section III. On the other hand, one can observe that the alarm signal is activated after 60 ms of the grid fault occurrence. This is due to the time needed by the voltage across the dc-bus capacitor to decrease under the specified threshold value. The latter was set to 0.9 i.e. $\frac{V_{on}^{Av}}{V_{dc}^{ref}/2} \leq 0.9$. This result emphasizes therefore the effectiveness of the proposed fault-detection method which is very simple and also insensitive to the chattering phenomenon

that affects the waveforms of the voltage across the faulty capacitor.

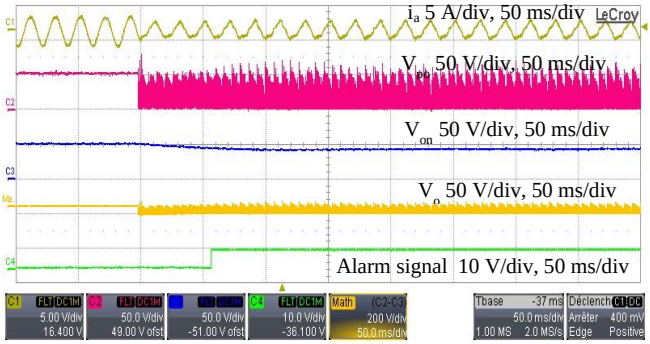

Fig. 8. From top to bottom: line current (ia), Vpo, Von, Vo, and alarm signal

V. Conclusion

A simple and efficient method was proposed with the aim to detect the open-circuit fault of the two capacitors in the dc-bus of a three-level NPC rectifier. The method divides the average value of voltage across each capacitor by the one of the dc-bus reference voltage. If for example the result related to the voltage across the lower capacitor decreases under a specified threshold value, therefore we can conclude that the fault affected the upper capacitor and vice-versa. The algorithm was implemented in real-time on a DSP controller and validated by experimental tests carried out on a laboratory prototype of the converter.

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