Low Power Low Jitter 0.18 CMOS Ring VCO Design with Strategy based on EKV3.0 Model

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***Abstract*—In this paper, the design of micro-power CMOS ring VCO with minimum jitter intended for a concept of frequency synthesizer in biotelemetry systems is studied. A design procedure implemented in MATLAB is described for a circuit realization with TSMC 0.18µm CMOS technology. This conventional design methodology based on EKV3.0 model is clearly suited to the challenges of analog circuits design with reduced channel width. Measures realized with ADS confirmed methodology capability to circuit sizing respecting the specifications of application. The designed ring VCO operates at a central frequency of 433MHz in ISM band with an amplitude of oscillation equal to 500 mV. The integration area was intrinsic (without buffers and without external capacitances). The simulated phase noise is about -108 dBc/Hz at 1MHz, the value of rms jitter is 44.8 ps and the power consumption of the designed VCO is 6.37 mW @ 433 MHz.**

Keywords*—Ring VCO; jitter; power consumption; EKV model; MATLAB

I. Introduction

An overview of some frequency synthesizers required for implantable biotelemetry systems cited in the literature would be presented in this section.

The full-divider frequency synthesizer shown in [1] generates two local oscillator (LO) signals at 1/3 and 2/3 of the central frequency of 5240 MHz. This fully integrated 0.25µm CMOS synthesizer includes a programmable loop filter and a VCO offering an 800 MHz adjustment range through a switchable capacitor bank. The synthesizer has a very low phase noise of -105 dBc / Hz at 10 kHz. However, this performance was accompanied by a very high power consumption of 93 mW.

A fully integrated synthesizer compatible with the ZigBee standard and implemented in a 0.18 µm CMOS process was presented in [2]. This circuit includes a third order passive loop filter. The VCO generates I/Q quadrature signals and the frequency divider was implemented using current-mode logic. The power consumption is 22 mW at a supply voltage of 1.8 V.

An entire divider CMOS synthesizer operating at 1 V supply voltage was presented in [3]. The VCO is based on the architecture implemented in 0.18 µm CMOS technology. The circuit uses a transformer in the feedback branch. Its power consumption is 10 mW. The measured phase noise is -139 dBc / Hz at 20 MHz from the carrier of 4.256 GHz. The synthesizer offers a tuning range of 4.114 to 4.352 GHz for 16 channels.

The synthesizer manufactured in 90-nm CMOS technology operating in the Industrial Scientific and Medical (ISM) band of 902-928 MHz was presented in [4]. This synthesizer based on a PLL allows the selection of seven channels and provides differential I/Q signals. The total measured consumption of the synthesizer is 640 µW.

Referring to the bibliography study, The VCO can be considered as the most important building blocks in the structure of frequency synthesizers based on the use of PLL. The VCO circuit is a critical component that significantly affects the performances of PLL in terms of phase noise, timing jitter and power consumption.

This work proposes a CMOS design of differential architecture of ring oscillator operating in ISM band. In Section II of this paper, the topology and characteristics of ring oscillators were exposed. In Section III of this paper, an innovative methodology approach based on EKV3.0 modeling for low power VC0 design was presented. Finally, simulations results and a comparative study with other works were exposed in Section IV.

II. Ring VCO Topology

The topology of the proposed VCO is based on the principle of cascading four delay cells with an inversion in the loop as shown in Fig. 1.

Each cell represents a differential nMOS pair (M5 and M6) with linear loads called Maneatis loads [5] consisting of the paralleling of a linear pMOS (M3 / M1) with a pMOS of the same size connected in a diode (M2 / M4) as shown in Fig. 2. The control of the oscillation frequency was realized as follows.

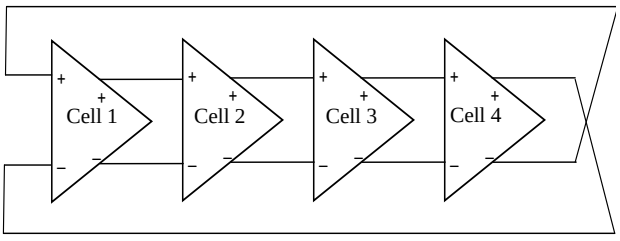

Fig. 1. Ring VCO topology.

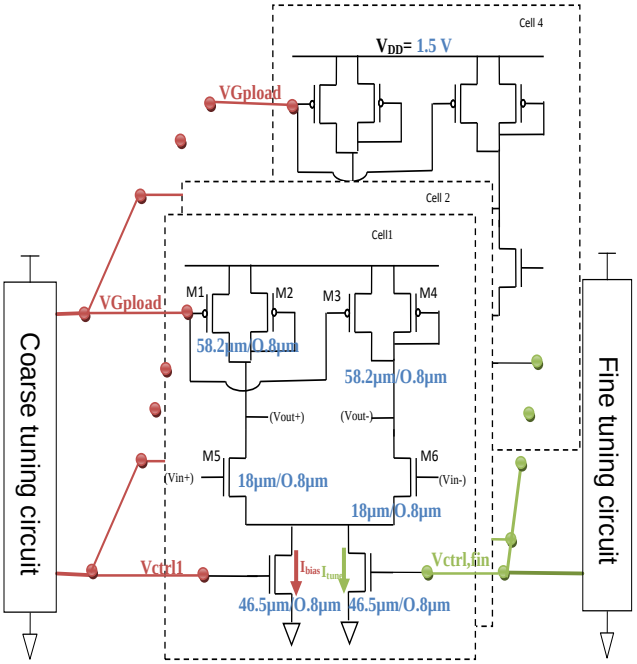

Fig. 2. Circuit of dual frequency - controlled CMOS ring VCO.

The coarse tuning circuit sets the gate voltage of the load pMOS V_{Gpload} so that with a current I_{bias} passing through the load, a voltage difference equal to V_{sw} occurs across its terminals representing the oscillation amplitude. This setting provides a wide frequency range by acting on the current I_{bias} while keeping V_{SW} constant.

The fine tuning circuit allows more precise control of the frequency by means of a differential voltage $V_{contrl,fin}$ controlling the injection of an additional current I_{tune} into each cell.

The expression of the oscillation frequency is given by:

$$f = \frac{1}{2\,N\,R_L\,C_m} \quad (1)$$

Where, N is the number of cells of the ring oscillator, R_L and C_m being respectively the equivalent resistance and capacitance seen at the output nodes.

The cell gain is computed as:

$$Av = g_{m,n}\,R_L = g_{m,n}\frac{V_{DD} - V_{outdc}}{I_{bias}/2} = \left(\frac{g_m}{I_D}\right)_n (V_{DD} - V_{outdc}) \quad (2)$$

Where, $g_{m,n}$ is the gate transconductance of nMOS transistor and V_{DD} is the supply voltage.

The expression of the VCO jitter is given by:

$$\overline{\Delta t_{VCO}}^2 = T_0\left(\frac{I_{bias}}{C_m V_{SW}}\right)\cdot\frac{KT\,C_m}{2\cdot(I_{bias})^2}\cdot(A_v\cdot\xi)^2 \quad (3)$$

Where, ξ represents noise factory contribution.

Notice that all capacitances and drain currents associated to transistors would be evaluated in the next section by the use of the EKV 3.0 model [6] giving continuous expressions from weak to strong inversion.

III. Dimensioning Algorithm of VCO

In this section, the modeling of the MOS transistor was developed by means of the EKV3.0 model [6].

Consider the half-pair of the differential cell to be dimensioned shown in Fig. 3 after replacing the current mirror by a constant current source delivering current I_B. The VCO differential cell sizing program was implemented on MATLAB following the design plan shown in Fig. 4. The design plan begins by setting the value of V_{DD} to reach. Then the resolution goes through a scan in dimensions to find the solutions compatible with the specifications. Here, an oscillation frequency equal to 433 MHz is required, the value of V_{SW} was fixed at 1 V and the gain of the cell Av was fixed at 1.5.

These parameters related to the circuit specifications were declared at the beginning of the program. The lengths of the transistors were also initialized to the same value 0.8µm.

This first step of data declaration ends with the introduction of some technological parameters of the transistors which were needed to evaluate the jitter, the intrinsic and extrinsic capacitances involved in the calculation of the total load capacitance seen at the output of the delay cell.

Now, using the results of the identification algorithm discussed in [7], the EKV parameters of the transistors were declared in a three-dimensional space (V_D, V_S, L). The sizing space in this program was defined in 2D by means of the log vectors q_{F1} and q_{F2} varying on a logarithmic scale.

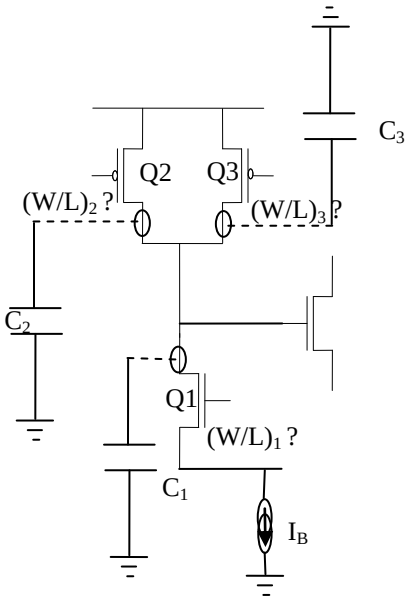

Fig. 3. The half-pair differential cell with equivalent capacitances seen at the output node.

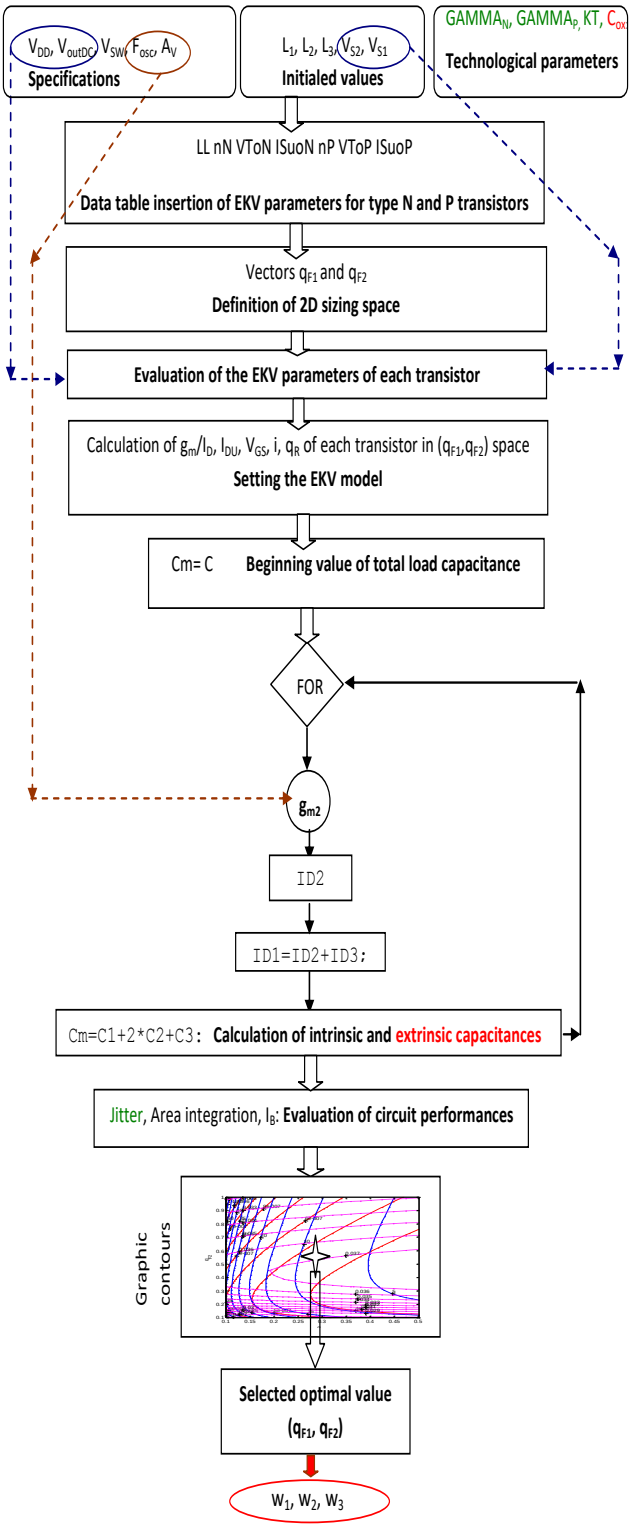

Fig. 4. Algorithm design for cell VCO dimensioning.

In the next step, the evaluation of the EKV parameters of each transistor in the dimensioning space was chosen according to their polarization levels. For the pMOS transistor Q2, the values of the source voltage and the drain-source voltage relative to V_{DD} were respectively 0V and V_{DD}-V_{outDC}. The normalized unit drain current I_{Du2} and V_{GS2} would be derived from the basic equations of the EKV model. The same approach is repeated for the transistor Q3 by takingV_{GS3} = V_{DS3} = V_{DS2}.

Similarly for the NMOS transistor Q1, it suffices to set V_{S1} to 0V and V_{DS1} to V_{outDC} to achieve I_{Du1} and V_{GS1}.

Once, all the EKV parameters of the transistors were placed in the dimensioning space, the procedure of finding the dimensions of the transistors according to the predefined specifications of the circuit would start. In this step, the design plan was inspired by the g_m/I_D methodology.

We begin by determining the value g_{m2} of the transistor Q2 from the gain of the cell and the oscillation frequency. The current of the drain I_{D2} of the transistor Q2 is subsequently deduced.

The ratio of the drain current I_{D2} to the unit current I_{DU2} designates the term $(W/L)_2$ = $(W/L)_3$. The values of the current I_{D3} were obtained referring to the empirical model. The sum of currents I_{D3} and I_{D2} gives the current I_{D1} from which the ratio $(W/L)_1$ is determined.

After determining the widths of the transistors, the program proceeds by calculating the intrinsic capacitances based on the EKV modelling and the extrinsic capacitances via the model developed in [8].

Finally, the calculation of the total load capacity seen at the output of the delay cell was established.

In the last step of this algorithm, the expressions of the circuit specifications as a function of q_{F1} and q_{F2} were introduced. Drawing the graphic contours of the jitter, the area integration and the bias current in the dimensioning space makes it possible to select a point (q_{F10}, q_{F20}) from which the optimal widths of transistors are determined.

At each solution, the performance of the circuit is calculated and the solutions can be selected according to the circuit specifications.

Fig. 5 illustrates the variation of the jitter (in red color) and the bias current (in blue) in the dimensioning space (q_{F1}, q_{F2}) for a cell gain equal to 1.5.

The selected point (q_{F10}, q_{F20}) from the dimensioning space allows the setting of jitter value at 7.5 10-11s and a bias current value of the order of 1mA. This point corresponds to a width of the pMOS transistors W_2 = W_3 = 57.4µm and to a width of the nMOS transistor W_1 = 18.2µm. These values will be retained in the simulation phase with the ADS tool.

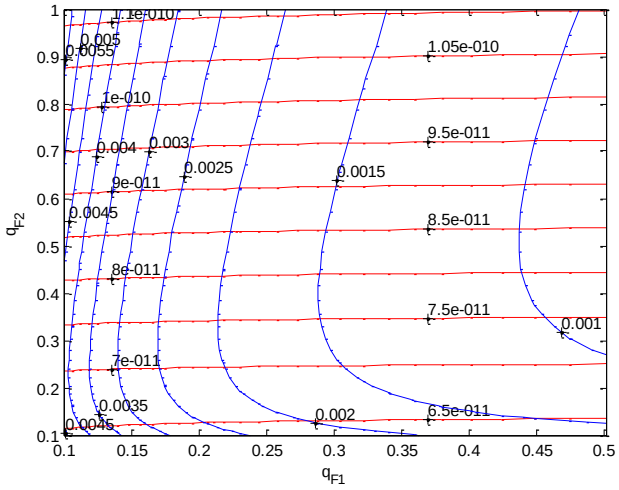

Fig. 5. Graphic contours of jitter and bias current.

IV. Simulation Results and Discussion

A. Simulation Results

The illustrated circuit of Fig. 2 was dimensioned in the previous paragraph for a realization with TSMC 0.18µm technology. In this part, simulations carried out on ADS environment were presented in order to characterize the designed ring VCO in terms of the circuit performances.

Fig. 6 shows the differential output signal Vout-diff obtained by transient analysis under ADS for a bias current I_B = 1mA. This signal oscillates at the desired frequency of 433 MHz with amplitude oscillation equal to 0.5 V. Fig. 7 shows the differential output signals for I_B = 500µA when the signal oscillates at the 374.5 MHz frequency maintaining the oscillation amplitude constant.

The evolution of the oscillation frequency as a function of the bias current I_B according to a coarse tuning control was presented in Table I. The tuning range was from 200 MHz to 450MHz. Table II shows the results of a fine tuning control of the VCO. The simulated gain sensibility of 11 MHz/V was achieved near the central frequency.

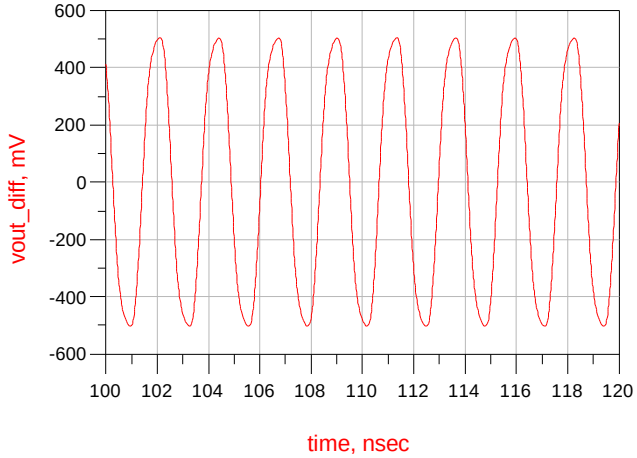

Fig. 6. Output signal for I_B = 1mA.

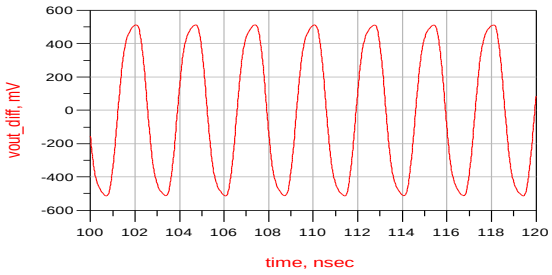

Fig. 7. Output signal for I_B = 500µA.

TABLE I. Frequency Oscillation as a Function of Bias Current

I_B (µA)	F_{osc} (MHz)
200	276.2
300	306.7
400	342.5
500	374.5
600	398.4
700	413.2
800	423.7
900	431
1000	432.9
1100	436.7
1300	442.5
1700	450.5

TABLE II. Frequency Oscillation as a Function of VCTRL, FIN

Vctrl,fin (V)	F_{osc} (MHz)
-0.75	413.2
-0.5	423.7
-0.25	431
0	432.9
0.25	434.8
0.5	436.7
0.75	438.6

Fig. 8 illustrates the simulated phase noise of the VCO through the Pnmx procedure using the harmonic balance method. The phase noise can be noticed as being equal to 107.9 dBC @ 1MHZ. The power consumption of the designed VCO is of the order of 6.37mW.

Finally, the use of the eye diagram available in ADS environment allowed us to calculate the temporal jitter of the circuit. Fig. 9 shows the eye diagram found for a VCO output signal oscillating at the 433MHz frequency. The value of the rms time jitter of the considered circuit is 4.48 10-11s.

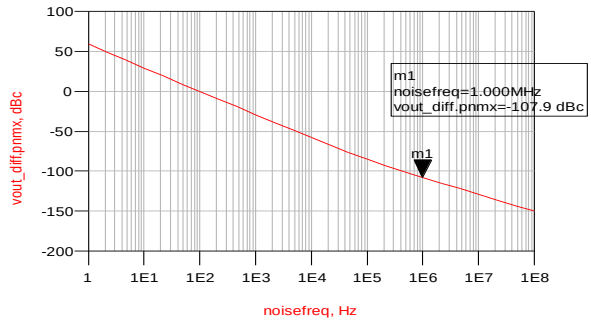

Fig. 8. Phase noise VCO curve.

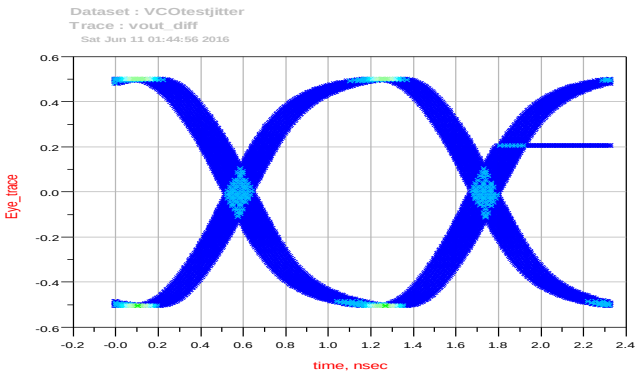

Fig. 9. Eye diagram for a VCO output @ 433MHz.

B. Compartive Study

Table III provide an overview of the performances of some existing ring VCO. The main fundamental characteristics given for each oscillator are: Technology, frequency coverage, power consumption and phase noise. It is not easy to make a comparison between these different structures as long as the technology used is not the same and as the parameters vary from one to the other. However, it is clear that achieving a high-performance VCO in terms of phase noise involves sacrificing other points such as consumption or favoring frequency coverage with a lower phase noise.

Most publications mentioned in Table III highlight a very high KVCO. Performances in terms of frequency coverage are certainly better, but the oscillator becomes very difficult to drive with a PLL and may create instability of the loop.

The advantage of the VCO realized in the framework of this work is to have a gain KVCO = 11MHz/V resulting from the use of a fine tuning control stage.

Opposite to this work, some circuits do not include the control module of the oscillation amplitude stability.

TABLE III. OVERVIEW OF SOME EXISTING RING VCO PERFORMANCES

Reference	N	Technology (µm)	Tuning range (GHz)	Power consumption (mw)	Phase noise (dBc/Hz)
[9]	3	0.35	0.381–1.15	7.48	−126
[10]	4	0.18	1.77–1.92	13	-123.4
[11]	3	0.18	0.479–4.09	10	−94.08
[12]	3	0.13	2.34–3.11	2	−113
[13]	4	0.065	485.7-1011	10	-110.8
This work	4	0.18	0.2-0.45	6.37	-107.9

The absence of this module certainly influences the quality of the modulation. Indeed, the variation of the control voltage will be followed not only by a frequency variation but also by a variation of the oscillation amplitude.

In addition, the use of external components in some publications like [9] gives qualities to the integrated circuits in terms of the consumption and noise performance of the circuits. The price to pay is the integration area. The power consumption of the VCO designed as part of this work is 6.37mW.

This circuit consumes less power compared to the circuits made in the other publications mentioned in Table III with the exception of [12] where the circuit was designed with 0.13 µ technology and powered by a 1.2 V value voltage.

V. CONCLUSION AND FUTURE WORK

In this paper, the design of dual frequency - controlled CMOS ring VCO was studied. An innovative methodology approach based on EKV3.0 modeling for low power VC0 design was presented. The VCO dimensioning algorithm developed with MATLAB was described for a circuit realization with TSMC 0.18µm CMOS technology. The results of simulations carried out under the ADS environment show that the circuit designed oscillates between 200 and 450 MHz with an amplitude of oscillation equal to 500mV. The simulated jitter is about 44.8ps and the power consumption of the designed VCO is 6.37mW at 433 MHz.

Therefore, the following benefits of this topology could be deduced:

- A high degree of integration considering that no passive element was used.
- A “natural” generation of the phase shift between the signals which leads to a high accuracy in phase and amplitude.
- Good frequency performance, which tends to improve markedly with the introduction of new low gate length CMOS technologies.

This last consideration therefore opens up prospects for our research work and shows that improvements can be made to the architecture presented by the use of advanced technologies. In addition, the future work will be interested to complete the design of the frequency synthesizer.

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