ROI-based Compression on Radiological Image by Urdhva-Tiryagbhyam and DWT Over FPGA

Suma
Research Scholar
Vidya Vikas Institute of Technology
Mysore, India

V. Sridhar
Principal, PES College of Engineering
Mandya
Karnataka, India

***Abstract*—The area of radiological image compression has not yet met its potential solution. After reviewing the existing mechanism of compression, it was found that majority of the existing techniques suffers from significant pitfalls e.g. more usage of transformation schemes, more resource utilization, delay, less focus on FPGA performance enhancement, extremely less emphasis on Vedic-multipliers. Hence, this paper presents an analytical modelling of ROI (Region of Interest)-based radiological image compression that applies Vedic Multiplier Urdhva-Tiryagbhyam to enhance the performance of coding using Discrete Wavelet Transform (DWT). The study outcome was implemented in Matlab and multiple test bed of FPGA devices (Virtex 4 FX100 -12 FF1152 and Spartan 3 XC400-5TQ144) and assessed using both visual and numerical outcomes to find that proposed system excel better performance in comparison to recently existing techniques.**

Keywords*—Radiological Image Compression; Discrete Wavelet Transform; FPGA; Lifting Scheme

I. INTRODUCTION

With the advancement of radiological image processing, the area of healthcare and the diagnostic sector has been imparted with various means to visualize the diseases with higher accuracies. Various kinds of radiological imaging systems e.g. Ultrasound, Positron Emission Tomography, Computed Tomography scans, Magnetic Resonance Imaging, have assisted radiologist and physician to investigate the disease very closely [1]. With the evolution of cloud, storage is never a problem and hence the adoption of cloud or any pervasive computing significantly assists in storing such radiological images. However, there is a darker side of this story even at present about radiological image. Normally, radiological images are very different from other types of images in the form of information contents. A normal MRI image can be around 5-6 MB, whereas the size can further increase [2]. Although storage is not a problem, a problem arises in particular applications e.g. telemedicine, robotic surgery, etc. [3][4][5]. In such applications, it is required that a bigger size of the image may need to be transferred from one to another end of the world with least delay as possible [6]. There are many network parameters e.g. traffic congestion, channel capacity, interference, noise that always affects the transmission [7], which is less likely to be controlled. However, a better transmission of a radiological image will also require that image retains its maximum signal quality which will degrade in the process of transmission. The solution of all this is an effective compression algorithm. An effective compression algorithm not only reduces the size but also ensures to retain maximum signal quality while reconstructing it at the end receiver [8]. At present, there are various lossless and lossy compression schemes [9] to accomplish maximized compression ratio, but the biggest challenge of lossy schemes is to recover the original data. On the other hand, usage of lossless compression schemes minimizes the compression ratio although it has the potential to recover the complete data. The significant problem is that lossless scheme is the only alternate solution in radiological image compression as it can't allow losing any forms of clinical information at any cost. Another problem is that bigger images e.g. MRI images has a bigger background which is not required to be processed at all as it occupies half of proportion size of the entire image resulting in the expensive matter. Moreover, such null background also has artifacts as well as noise during the process of acquisition of an image. Hence, implementation of denoising techniques further degrades the signal quality [10]. At present, there is an increasing trend of using JPEG2000 standards owing to its supportability of advanced characteristics of radiological image processing. It is found to have an optimal efficiency of coding in comparison to conventional compression scheme [11]. JPEG2000 also has higher supportable features of Discrete Wavelet Transform (DWT) along with various arithmetical schemes of coding [12]. There is an increasing attention from the research community towards using DWT-based scheme and its associated architecture. It was also found that FPGA has enough potential to hone the potential features of DWT. There have been a various research attempts on using FPGA and DWT together in image processing [13]. All these implementations suffer from certain flaws e.g. more dependencies on control signals, inferior hardware utilization, more latency, increasing demands of registers in hardware design, etc. This paper introduces a technique that jointly uses Vedic Multiplier, FPGA (Field Programmable Gate Array), lifting scheme, and DWT (Discrete Wavelet Transform) to overcome the problems. Section II discusses the existing research work towards the topic followed by a briefing of problem identification in Section III. Section IV introduces the adopted methodology of proposed system followed by a discussion of algorithms in Section V. Result accomplished from the study is discussed in section VI followed by a summary of the work in conclusion under Section VII.

II. RELATED WORK

This section discusses the techniques adopted for radiological image compression during the year 2010-2015.

Discrete Cosine Transform is one of the most frequently used compression algorithm for images. The work carried out by Dhandapani and Ramachandran [14] have presented an 8x8 transformation matrix needed by an added and thereby skipping shift and multiplication using FPGA. Although, the outcome was found to exhibit power effectiveness with lesser delay compared to other existing system but it doesn't prove computational efficiency. Another frequently used technique to perform compression is DWT and SPIHT (Set-Partitioning in Hierarchical Trees). Fang et al. [15] have introduced a unique interpolation-based scheme using Lagrangian theory in to show better supportability of prediction depending upon local features. The study outcome was found to minimize execution time along with the length of coding bits but was not found to offer better signal quality of reconstructed image. Usage of DWT for radiological image compression was also seen in the work of Govindan and Sanile [16], where it was used for truncating the sub-bands in ultrasonic images. The authors have also applied interpolation technique using Fourier transform to obtain enhanced signal quality. The study has used both spatial and temporal correlational properties in to perform compression. The study outcome was assessed to find better signal quality (measured by PSNR), correlational coefficient, and quality of reconstruction, computational speed, and resource utilization. However, the technique was not found benchmarked. Same authors [17] have extended the similar work using system-on-chip platform using OpenCL language over GPU. Medical images are not only limited to radiological images, but there are also other forms of it. One of such form is DNA microarray, which is frequently used in genetic engineering. Cabronero et al. [18] have particularly addressed the problem of compressing such medical image of DNA microarray using a quantization-based approach. The contribution of the work is to restrict the relative error due to quantization. On increasing bitrates, the study was found to have better error control. Rehman et al. [19] have presented a discussion on bi-orthogonal transform. The technique takes the input image and converts it to macro blocks which are then further transformed into blocks and pixels. The authors have used JPEG XR to perform compression with lowered memory usage. Yoon et al. [20] have applied L-fold down sampling to minimize the coefficients of filters and data rates.

Apart from transform-based implementation techniques, there is a frequent usage of FPGA-based schemes too for performing compression. Ahmad et al. [21] have introduced a three-dimensional daubechies for compressing the medical image. The three dimensionalities are achieved by considering two transpose buffers and one-dimensional Daubechies. The study outcome was found with lower consumption of power but without benchmarking. Anjaneyulu and Krishna [22] have used conventional DWT as well as SPIHT on FPGA. However, this work is a replica of original work carried out by Fang et al. [15] and doesn't show many novel features in work. Usage of FPGA was also advocated by Botella et al. [23]. In existing system, FPGA was used in a different way too. For example, the work carried out by Li et al. [24] has developed a synthesis tool using FPGA. However, the study didn't provide enough evidence to claim its effectiveness. Nagabhushanam et al. [25] has also used FPGA-based approach and DWT-based scheme to perform image compression. The authors have addressed the complexity of DWT by incorporating the enhanced version of DWT using distributive arithmetic. The study outcome was found with lowered latency and increased throughput regarding clock cycles. However, the outcome didn't studied computational complexity. Wu et al. [26] have applied SPIHT along with FPGA to perform image compression. The technique incorporates parallelism over SPIHT algorithm to enhance the processing capacity. The basic technique is to retain the maximized PSNR and minimize the storage demands. However, the technique is not cost effective if the dataset is changed to complex medical image. Xuesen et al. [27] have designed an experimental test-bed that uses FPGA for investigating the acquired data from the medical image.

Among all these techniques, the performance of the system can be greatly enhanced if a suitable multiplier is applied to maintain a balance between compression and quality of the reconstructed image. In this regards, Vedic-based multipliers designs have also been researched to some extent. Most recently, Arish and Sharma [28] have presented a design of multiplier for floating point that significantly controls both power dissipation and delay. The authors have used two Vedic-based schemes e.g. Urdhva-Tiryagbhyam algorithm and Karatsuba algorithm to deploy binary multiplier of the unsigned type for the purpose of carrying out mantissa multiplication. An exactly similar version of work is also carried out by Kodali et al. [29] in the same year. Usage of Vedic mathematics was found in work carried out by Pohokar et al. [30]. The work was carried out in FPGA and outcomes are found with reduced delay and memory demands compared to the traditional multiplier. Nearly similar work was also carried out by Sharma and Goyal [31] most recently only with a difference that actual work of Pohokar [30] was implemented in FPGA in 2015 and same work was also published by Sharma and Goyal [31] in H-Spice in 2016. Singh and Sasamal [32] have presented a study where binary Vedic multiplier is implemented over cadence tool using adiabatic logic. Usage of another Vedic sutra called as Calana Kalanabhyam was seen in the work of Verma et al. [33] where the authors have used it alongside with FPGA to make energy-efficient sutra. Vijayan et al. [34] have presented a Vedic multiplier of 8-bits in FPGA. Hence, it can be seen that there are quite a lot of study being carried out on the topic of image compression using DCT, Fourier transforms, FPGA, Vedic multiplier, SPIHT, etc. All the studies have significant points to learn as well as pitfalls too. The Vedic multiplier, although being an older concept, has not been much explored in the area of medical image compression. The next section elaborates about the problems being identified from the existing studies.

III. PROBLEM IDENTIFICATION

This section discusses the problem identification after reviewing the literature from the existing system:

- **More inclination towards transformation-based schemes**: It has also been seen that transformation based schemes (e.g. DWT, DCT, SPIHT) are more used for performing compression. However, there is some potential trade-off in using such schemes which were completely not highlighted in any of the research work till date. Although wavelet-based schemes

support compression of both lossy and lossless image, unfortunately there are many modalities that are found not support the generation of compressed objects in JPEG2000 [35]. Existing techniques doesn't addressed a problem that compressed JPEG2000 objects are not supported by Picture Archiving And Communication System (PACS) that forces converting the image to some other formats while transmission. Moreover, usage of the wavelet-based scheme includes higher computational cost [35].

- **Less focus on enhancing FPGA**: At present, there are many FPGA-based schemes using radiological image processing. However, the biggest research gap is FPGA is just used as a platform for synthesis. For example, the work carried out by various researchers [24][25][26] have used FPGA using an image. However, it was totally ignored that image conversion module over various devices of FPGA includes various steps that are a computationally intensive process. There are also studies that have used FPGA and DWT for image compression using distributed arithmetic which includes increasing number of shift registers on LUT. The techniques using DWT and FPGA cannot optimize the entropy encoding.
- **Less Emphasis on Vedic Multipliers**: There are only 2 transaction papers and 155 conference papers on Vedic-based approaches published during 2010-2016 in IEEE Xplore. However, about radiological image compression, there exist only two conference papers that have implemented Vedic multiplier during last 5 years [36][37]. This itself is one of the potential evidence that there has been quite a less emphasis on standard research work towards realizing the potential characteristics of Vedic-based approaches in medical image compression.

Apart from the above-mentioned problems, it was also found that existing techniques suffers from certain common problem viz. i) lack of benchmarking, ii) inappropriate architecture usage leading to poor process of image reconstruction, ii) considers the entire image for compression leading to more bandwidth utilization as well as computational resource utilization, etc. Moreover, the potential of the Vedic multiplier, DWT and FPGA are less explored jointly. Hence, the problem statement can be stated as "*It is a challenging task to develop a faster radiological image compression considering the joint potential of DWT, FPGA, and Vedic Multipliers.*" The next section about the methodology adopted in to address the identified problems.

IV. Proposed Methodology

The design and implementation of the proposed work are carried out using analytical-based methodology. The present work is a continuation of our prior works [36][38][39]. The proposed system implements Vedic multiplier called as *Urdhva-Tiryagbhyam*. The beneficial point of this multiplier is that it can concurrently handle addition and fractional product generation. This feature gives more edge to parallel processing that can significantly reduce the delay time. It also makes it highly suitable for performing binary multiplication. Fig.1 highlights the architecture designed for the proposed system.

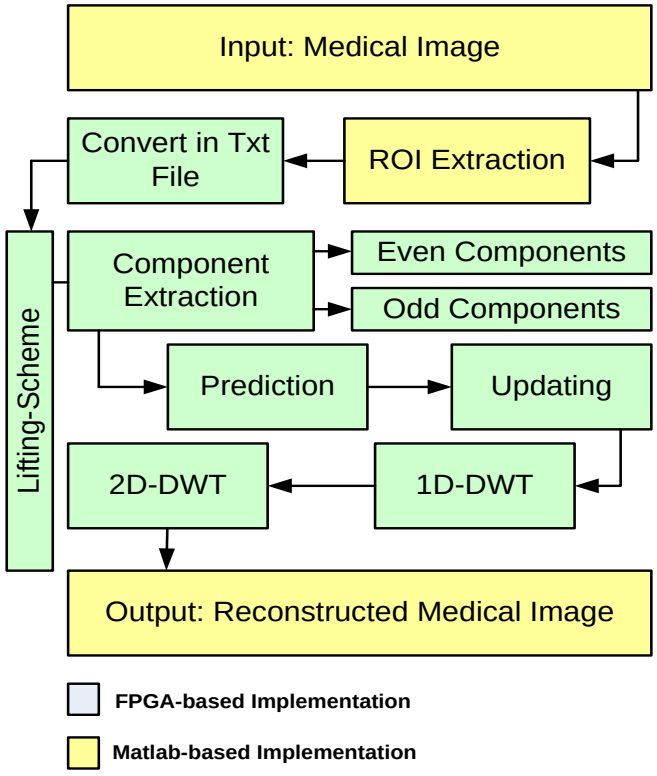

Fig. 1. Proposed Methodology

The proposed system uses Region-of-Interest for taking the input of radiological image, which means the proposed algorithm is only applicable to ROI and not the complete radiological image. It than converts the image into a binary text file, so that it can be processed effectively in FPGA. The next step is to apply lifting scheme which has its inherent advantages over eliminating redundancies. It works by classifying the ROI data to even and odd samples further followed by prediction and updating operation. Prediction process assists in obtaining approximated coefficients while updating operation assists in obtaining detailed coefficient values. This step is carried out to resist lossy data and to obtained lossless data during the entire process of radiological image compression. Finally, it generates high and loss pass components of one-dimensional DWT which is further processed back to obtain two-dimensional DWT in the form of a reconstructed image. The elaborated discussion of the algorithm of proposed system is carried out in next section.

V. Algorithm Implementation

The main purpose of this algorithm is to perform radiological image compression using the Vedic multiplier. The proposed system uses radiological image database of [40] in algorithm implementation. In spite of compressing the entire image, we choose to compress only the Region-of-Interest (ROI). The advantage is faster processing, less allocation of computational resources, and retention of the image portion of clinical importance. The proposed system uses Matlab to take the input of radiological image and then convert it into a text

file (a form of a hexadecimal number), which is further subjected to FPGA (Line-2). The entire algorithm implementation is carried out over FPGA itself. It is already known that a filtering operation can be carried out over DWT that can be represented as,

$$M(i)=\prod_{j=1}^{m}\begin{pmatrix} TL_e(i) & TH_e(i) \\ TL_o(i) & TH_o(i) \end{pmatrix} \quad (1)$$

In the above equation, $TL(i)$ and $TL(i)$ corresponds to transfer function of low as well as high pass filter. It also means that $TL_e(i)$ and $TH_e(i)$ corresponds to even components while $TL_o(i)$ and $TH_o(i)$ represents odd components. The better representation of the transform function could be,

$$(\varphi(i) \quad \theta(i)) = (x_e(i) \quad \frac{1}{z}x_o(i))M(i) \quad (2)$$

In the above equation, the variables $\varphi(i)$ and $\theta(i)$ represents both low and high pass components that have been filtered from its input signal $x(i)$. The proposed system also uses lifting scheme that can further factorize the matrix representation giving better feasibility to enhancing the capability of the processor. Another advantage of applying lifting scheme will be to eliminate the redundancies. As per Fig.2, even clocking will be functional on the registers position on top while odd clocking will be operational for the registers positioned on the bottom. Using a clock cycle of a unit pixel, the ROI image data is fed in serial order to classify the data as even (c_e) and odd components (c_o) (Line-3). This operation will lead to the implementation of lifting scheme that further results in low pass components (LP_c) and high pass components (HP_c) (Line-4). A unit of low pass coefficient, as well as high pass coefficient will be generated for a single unit of ROI image.

Algorithm for Compressing Radiological Image

Input: I_{roi} (image), c_e / c_o (even and odd component), LP_c / HP_c (Low and High pass components)

Output: I_{recon} (reconstructed image)

Start

1. init ()
2. read I_{roi}, I_{roi}→txt()
3. [α, β]=classify(txt)→[c_e, c_o]
4. get()=[LP_c, HP_c]
5. get()→(x_5[n], x_6[n])→1D DWT
6. Apply Urdhva-Tiryagbhyam
7. I_{recon}=get(txt)← 2D DWT

End

The generated low pass component and high pass components are then identified. The proposed system also makes use of Daubechies 9/7 filters. The advantage will be an enhancement in the compression performance will be retained to maximum level with proper control over computational complexity. This implementation policy can be seen in Fig.1, where the ROI image data is forwarded through numerous steps. The numbers of transformed coefficients are retained to be similar as that of original one owing to sub-sampling. The system than processes the data to obtain detailed (x_5(i)) and approximation coefficients (x_6(i)) of one-dimensional DWT (Line-5). Implemented over FPGA using Verilog, the coefficient outcome was obtained.

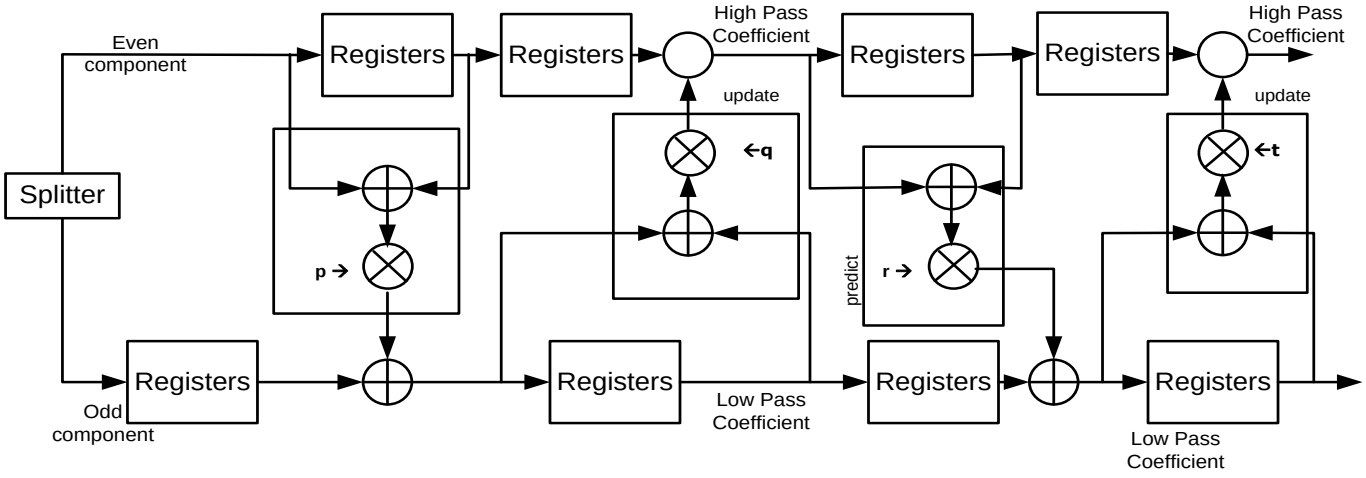

Fig. 2. Algorithm Operations in DWT

The next part of the algorithm implementation is to apply Vedic multiplier design using hardware-based architectural approach (Line-6). The implemented design scheme of the Vedic multiplier was shown in Fig.3.

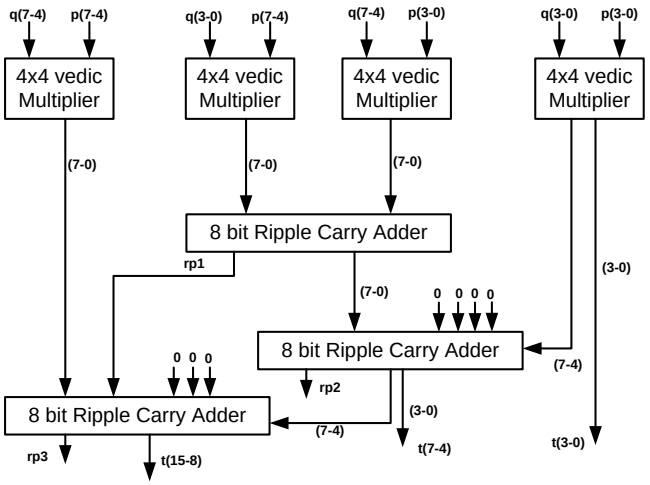

Fig. 3. 8x8 Vedic Multiplier Design

The proposed technique has been testified for both 2x2 as well as a 4x4 bit of Vedic multiplier to design the hardware architecture. The system uses Urdhva Tiryagbhyam sutra which is meant for vertical and crosswise multiplication of dual-number of binary origin. Initially a 4x4 bit of Vedic multiplier has been designed, which further uses 8 bit of ripple carry added to formulate an 8x8 bit of Vedic multiplier. The entire process starts with 2 bit numbers say P and Q to for 2x2 bit of Vedic multiplier using vertical and crosswise multiplication of least significant bits. It is then enhanced with 4x4 bit of Vedic multiplier considering two-bit at a time in 2-bit block of the multiplier. Although, it can reduce delay, the delay performance can be further enhanced by considering four 4x4 bit of Vedic multiplier and three 8 bit of ripple carry adder. Consider $P=P_7\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$ and $Q=Q_7\ Q_6\ Q_5\ Q_4\ Q_3\ Q_2\ Q_1\ Q_0$. Therefore, according to the concept of Vedic-based multiplication, it will result in 16 bits as $T_{15}\ T_{14}\ T_{13}\ T_{12}\ T_{11}\ T_{10}\ T_9\ T_8\ T_7\ T_6\ T_5\ T_4\ T_3\ T_2\ T_1\ T_0$. Dividing the bits P and Q will result in further decomposition into a pair of minimum 4 bits of sub-bits e.g. P_{high} and P_{low}. Similar generation will be yield by Q also as Q_{high} and $Q_{low.}$ The further processing of multiplication is carried out by utilizing 4 bits of multiplier blocks and considering 4 bits at a single instance, which is by the Vedic multiplier theorem of Urdhva Tiryagbhyam sutra. Finally, the resultant is accomplished from the addition of the multipliers of 4x4 bit output. In this entire process, three ripple carrier adders of 8 bits are also used as shown in Fig.3. The final-outcome from the FPGA is than fed to Matlab to obtain a reconstructed image (Line-7). Hence, the proposed system wisely utilizes the Vedic multiplier to enhance the compression performance over radiological images. The next section discusses the results being accomplished by the implementation of the algorithm discussed in this section.

VI. Result Discussion

The proposed system was implemented on 32 bit windows system with normal 4 GB of RAM and core-i5 processor. The implementation is carried out over two types of FPGA devices i.e. i) Virtex 4 FX100 -12 FF1152 and ii) Spartan 3 XC400-5TQ144. The formation of the one-dimensional DWT with Vedic multiplier using Xilinx and Verilog is shown in Fig.4

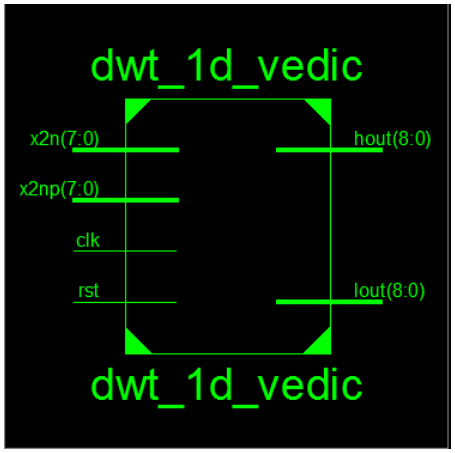

Fig. 4. Module of 1D_DWT

Upon receiving the input data, it is classified in even and odd components which are then reposited in registers. The registers will have a null value when there is higher reset, but during lower reset, the registers classify the input ROI image in the form of odd and even components. The lifting schemes enable to read the input ROI data to 16 clock cycles whereas the resultant outcome will have both high and low pass components according to the algorithm steps (one-dimensional-DWT). The module shown in Fig.4 takes the input of pixel values, which categorizes the values in odd and even components and develops a matrix where it is stored. This operation is then followed by the Vedic multiplier to further leverage the compression process.

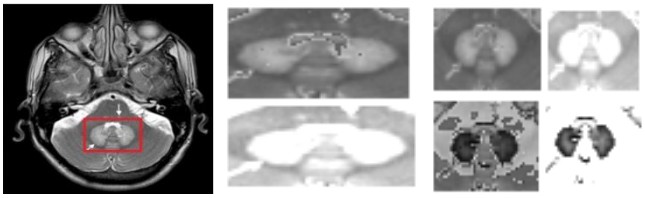

Fig. 5. (a) Input image (b) 1D-DWT results (c) 2D-DWT results

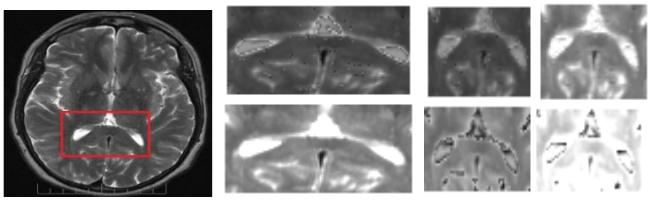

Fig. 6. (a) Input image (b) 1D-DWT results (c) 2D-DWT results

Fig. 5-6 shows the visual outcomes of the two sample radiological image whose ROI is considered for performing compression operation using proposed system. Both the visual outcomes show accomplishment of one-dimensional DWT outcomes, which is then followed by two-dimensional DWT outcomes. A closer look at the reconstructed two-dimensional DWT image shows better perceptibility of the processed radiological image after applying compression.

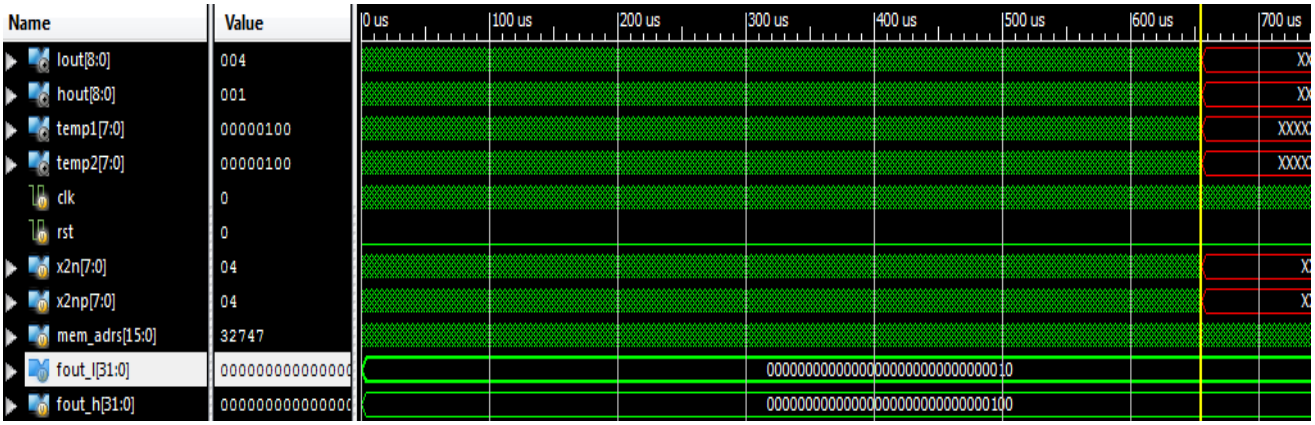

Fig. 7. Simulation results of 2D-DWT

Fig.7 highlights the simulation outcome of two dimensional DWT in FPGA. For effective analysis, the design of the proposed system is compared with the similar type of work presented by Todkar [41] and Mhamunkar [42] most recently. The standard performance parameters are retained e.g. logic utilization, number of slices, number of slice flip flops, number of 4 unit LUT, and number of bonded IOBs.

The work carried out by Todkar [41] was mainly focused on enhancing the operation of two dimensional DWT over VLSI-based architecture. The authors have used 9/7 filter design as the lifting scheme that is quite similar to us. The technique has minimized the higher dependencies of registers to have better control over a delay. The authors have amended the design of DWT, transpose unit, processing elements, and mechanism of prediction and update. The implementation was carried out using 16 multipliers, 5 input buffers, 54 registers, 24 adders, and 11 transposition registers with lifting based DWT scheme. The numerical outcome was presented in Table 1 using FPGA device (Virtex 4 FX100 -12 FF1152).

TABLE I. NUMERICAL COMPARATIVE ANALYSIS-I

		Proposed Design		Todkar's approach [41]	
Logic Utilization	Available	Used	Utilization	Used	Utilization
Number of Slices	42176	770	1%	878	2%
Number of Slice Flip Flops	84352	295	0%	1072	1%
Number of 4 input LUTs	84352	1394	1%	1263	1%
Number of bonded IOBs	576	36	6%	NA	6%
Number of GCLKs	32	1	3%	1	3%

The first significant improvement can be seen is the lowered dependencies on the utilization of slices by proposed system and it almost doesn't use any flip flops. The complete processing time of the algorithm for proposed system is found to be 47% improved as compared to Todkar's approach [41] with less computational complexity

TABLE II. NUMERICAL COMPARATIVE ANALYSIS-I

		Proposed Design		Mhamunkar's approach [42]	
Logic Utilization	Available	Used	Utilization	Used	Utilization
Number of Slices	1920	742	38%	1880	97%
Number of Slice Flip Flops	3840	295	7%	2118	55%
Number of 4 input LUTs	3840	1340	34%	2971	77%
Number of bonded IOBs	97	36	37%	62	63%
Number of GCLKs	8	1	12%	4	50%

The above Table 2 shows the numerical analysis of proposed system with that of work carried out by Mhamunkar [42]. The author have used frequently used image compression algorithm i.e. SPIHT with an objective to maintain balance between compression and image quality over FPGA. The algorithm processes the input image in order to extract the header files and deployed hardware customer logic and used micro blaze processor over FPGA to perform SPIHT encoding and decoding. We have maintained the similar environment of implementation by considering the equivalent FPGA device (Spartan 3 XC400-5TQ144). The result shows that there is a considerable amount of improvement in all the performance parameters of proposed system in contrast to the recent work carried out by Mhamunkar [42].

The proposed system takes the odd and even components after it explores the high signal load in order to deploy it for generating low pass coefficients. This operation is exponentially speeded up by using enhanced Vedic multiplier, which has the further capability to minimize area as well as delay as compared to any traditional mechanism of radiological image compression. During the entire observation, it was found that proposed system has significantly lowered the dependencies on full adder as well as a half adder in comparison to usage of ripple carry adder. Implementation of DWT-based approach has further ensured retention of the maximum degree of signal quality of the reconstructed image.

VII. Conclusion

This research paper has presented an idea of performing compression of radiological images. Even after decades of research work towards image compression, this field has not witnessed a robust compression algorithm yet. In spite of availability of various compression schemes, the applicability of them in medical images are quite less owing to its dependencies on lossless compression scheme. After reviewing literature, it was explored that usage of DWT along with lifting schemes and FPGA are good possibilities to accomplish such lossless data during compression. Further, it was also found that potential characteristics of Vedic multipliers towards addressing the problems in compression are also left untapped in existing research work. Hence, a novel techniques have been discussed that jointly utilizes DWT, FPGA, and Vedic multiplier to accomplish an objective of cost-effective medical image compression. Our outcomes are also compared with similar kinds of schemes being recently published to find that proposed system exhibits a better balance between compression and image quality.

References

[1] J. R. Haaga, D. Boll, Computed Tomography & Magnetic Resonance Imaging Of The Whole Body, Elsevier Health Sciences, 2016

[2] http://www.telemedproviders.com/telemedicine-articles/91-magnetic-resonance-imaging-mri.html

[3] H. Eren, J. G. Webster, Telemedicine and Electronic Medicine, CRC Press, 2015

[4] https://www.doc.ic.ac.uk/~nd/surprise_96/journal/vol4/ao2/report.html

[5] S. Avgousti, E. G. Christoforou, A. S. Panayides, S. Voskarides, C. Novales, L. Nouaille, C. S. Pattichis and P. Vieyres, "Medical telerobotic systems: current status and future trends", BioMedical Engineering OnLine, 2016, DOI: 10.1186/s12938-016-0217-7

[6] M. J. Khan, A. Bhattacharyya, M. Alam, "Design Issues And Challenges Of Reliable And Secure Transmission Of Medical Images", *eSAT Journals*, 2016, DOI: http://doi.org/10.15623/ijret.2014.0322034

[7] J. Ramsden, Bioinformatics: An Introduction, Springer, pp.34, 2015

[8] W. Kou, Digital Image Compression: Algorithms and Standards, Springer Science & Business Media, 2013

[9] M. El-Ghoboushi, Comparison of Lossless Image Compression Techniques based on Context Modeling, GRIN Verlag, 2015

[10] S. Gupta and Meenakshi, "A review and comprehensive comparison of image denoising techniques," *IEEE International Conference on Computing for Sustainable Global Development* (INDIACom), New Delhi, 2014, pp. 972-976, 2014

[11] D. Taubman, M. Marcellin, "JPEG2000 Image Compression Fundamentals, Standards and Practice: Image Compression Fundamentals, Standards and Practice, Springer Science & Business Media, 2012

[12] P. V. Fleet, Discrete Wavelet Transformations: An Elementary Approach with Applications, John Wiley & Sons, 2011

[13] S-C Ou, H-Y Chung, W-T Sung, "Improving the compression and encryption of images using FPGA-based cryptosystems", *Springer-Multimedia Tools and Applications*, vol.28, Iss.1, pp.5-22, 2006

[14] V. Dhandapani and S. Ramachandran, "Area and power efficient DCT architecture for image compression", *Springer- EURASIP Journal on Advances in Signal Processing*, 2014

[15] Z. Fang, N. Xiong, L. T. Yang, X. Sun, and Y. Yang, "Interpolation-Based Direction-Adaptive Lifting DWT and Modified SPIHT for Image Compression in Multimedia Communications", *IEEE Systems Journal*, Vol. 5, No. 4, December 2011

[16] P. Govindan, J. Saniie, "Processing algorithms for three-dimensional data compression of ultrasonic radio frequency signals", *IEEE- IET Signal Processing*, Vol. 9, Iss. 3, pp. 267–276, 2015

[17] P. Govindan, B. Wang, P. Ravi, J. Saniie, "Hardware and software architectures for computationally efficient three-dimensional ultrasonic data compression", *IEEE- IET Circuits, Devices & Systems*, pp.1-8, 2015

[18] M. H. Cabronero, I. Blanes, A. J. Pinho, M. W. Marcellin, J. S. Sagrista, "Analysis-Driven Lossy Compression of DNA Microarray Images", *IEEE Transactions on Medical Imaging*, 2015

[19] M. R. Rehman, G. Raja and A. K. Khan, "Implementation of Lapped Biorthogonal Transform for JPEG-XR Image Coding", *Intech Open Science*, 2012

[20] C. Yoon, W. Lee, J. H. Chang, T-K Song, and Y. Yoo, "An Efficient Pulse Compression Method of Chirp-Coded Excitation in Medical Ultrasound Imaging", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 60, no. 10, October 2013

[21] A. Ahmad, N. H. Jaafar, A. Amira, "FPGA-based Implementation of 3-D Daubechies for Medical Image Compression", *EMBS Conference on Biomedical Engineering and Sciences*, pp.683-688, 2012

[22] I. V. Anjaneyulu, P. R. Krishna, "FPGA Implementation of DWT-SPIHT Algorithm For Image Compression", *International Journal Of Technology Enhancements And Emerging Engineering Research*, Vol 2, Iss.3, 2014

[23] G. Botella, C. García, and U. M. Base, "Hardware implementation of machine vision systems: image and video processing", *Springer-EURASIP Journal on Advances in Signal Processing*, vol.152, 2013.

[24] Y. Li, W. Jia, B. Luan, Z-H Mao, H Zhang, M. Sun, "A FPGA Implementation of JPEG Baseline Encoder for Wearable Devices", *41st Annual Northeast Biomedical Engineering Conference (NEBEC)*, pp.1-2, 2015

[25] M. Nagabushanam, C. P. Raj, S. Ramachandran, "Design and FPGA Implementation of Modified Distributive Arithmetic Based DWT – IDWT Processor for Image Compression", *IEEE International Conference on Communications and Signal Processing*, pp.1-4, 2011

[26] Y-H Wu, Y-H Wu, L-X Jin, H-J Tao, "An improved fast parallel SPIHT algorithm and its FPGA implementation", *2nd International Conference on Future Computer and Communication*, pp.191-195, 2010

[27] C. Xuesen, H. Liguo, D. Jinbo, "Design and implementation of FPGA-base diagnosis of medical image data acquisition equipment", *IEEE-The Tenth International Conference on Electronic Measurement & Instruments*, pp.51-55, 2011

[28] Arish S, R.K.Sharma, "An efficient floating point multiplier design for high speed applications using Karatsuba algorithm and Urdhva-Tiryagbhyam algorithm", *IEEE Global Conference on Communication Technologies*, pp.192-196, 2015

[29] R. K. Kodali, L. Boppana and S. S. Yenamachintala, "FPGA Implementation of Vedic Floating Point Multiplier", *IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems*, pp.1-4, 2015

[30] S.P.Pohokar, R.S.Sisal, K.M.Gaikwad, M.M.Patil, R. Borse, "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics", *International Conference on Industrial Instrumentation and Control*, 2015

[31] J. Sharma, C.Goyal, "High Speed 16- Bit Vedic Multiplier Using Modified Carry Select Adder", *An International Journal of Engineering Sciences*, Vol. 17, 2016

[32] S. Singh, T. N. Sasamal, "Design of Vedic Multiplier using Adiabatic Logic", *IEEE International Conference on Futuristic trend in Computational Analysis and Knowledge Management*, 2015

[33] G. Verma, S. Shekhar, K. S. Kant, V. Verma, H. Verma, and B Pandey, "SSTL IO Standard Based Low Power Arithmetic Design Using Calana Kalanabhyam On FPGA", *International Journal of Control and Automation*, Vol. 9, No. 4, pp. 271-278, 2016

[34] A. E Vijayan, A. John, D. Sen, "Efficient Implementation of 8-bit Vedic Multipliers for Image Processing Application", *IEEE International Conference on Contemporary Computing and Informatics*, pp.544-552, 2014

[35] D. Dennison and K. Ho, "Informatics Challenges—Lossy Compression in Medical Imaging", *PMC-US National Library of Medicine, National Institutes of Health, Journal fo Digital Imaging*, vol.27, Iss.3, pp.287-291, 2014. 10.1007/s10278-014-9693-0

[36] S. Ravishkumar, V. Sridhar, "VCAR: Vedic Compression Algorithm Over Region of Interest on Radiological Image", *IEEEInternational Conference on Emerging Research in Electronics, Computer Science and Technology*, 2015

[37] S. S. Kerur, P. Narchi, H. M Kittur, Girish V. A, "Implementation of Vedic Multiplier in Image Compression using DCT Algorithm", *IEEE 2nd International Conference on Devices, Circuits and Systems*, 2014

[38] S. Ravishkumar, V Sridhar, "Computational Modelling of Image Coding using ROI based Medical Image Compression", *International Journal of Computer Applications*, Vol.108, No. 5, December 2014

[39] S. Ravishkumar, V. Sridhar, "Design of Multiplier for Medical Image Compression Using Urdhava Tiryakbhyam Sutra", *International Journal of Electrical and Computer Engineering* (Scopus-indexed), vol.6, No.3, 2016

[40] "Public Image Databases", Cornell University Vision and Image Analysis Group, Retrieved, 12 july, 2016, Link:- http://www.via.cornell.edu/databases/

[41] S. Todkar, P.V.S. Shastry, "Flipping Based High Performance Pipelined VLSI Architecture for 2-D Discrete Wavelet Transform", *IEEE International Conference on Applied and Theoretical Computing and Communication Technology*, 2015

[42] N. S. Mhamunkar, B. S. Gayal, "Design And Implementation Of GENERIC 2-D Biorthogonal Discrete Wavelet Transform On FPGA", *IEEE International Conference on Energy Systems and Applications*, 2015