Design of 1-bit Comparator using 2 Dot 1 Electron Quantum-Dot Cellular Automata

Angona Sarker
Dept. of Information and Communication Technology
Mawlana Bhashani Science and Technology University
Tangail, Bangladesh

Md. Badrul Alam Miah
Dept. of Information and Communication Technology
Mawlana Bhashani Science and Technology University
Tangail, Bangladesh

Ali Newaz Bahar
Dept. of Information and Communication Technology
Mawlana Bhashani Science and Technology University
Tangail, Bangladesh

***Abstract*—In nanotechnologies, quantum-dot cellular automata (QCA) offer promising and attractive features for nano-scale computing. QCA effectively overcomes the scaling shortfalls of CMOS technology. One of the variants of QCA is 4 Dot 2 Electron QCA which is well explored and researched. The main concentration of this study is on 2 Dot 1 Electron QCA, an emerging variant of QCA. A novel and efficient XOR gate based on 2 Dot 1 Electron QCA is designed. Moreover a comparator using the proposed novel XOR gate is presented in this present scope. The proposed architecture is justified using a well-accepted standard mathematical function based on Coulomb's law. Energy and power dissipation of the architecture are analyzed using different energy parameters. AS the compactness of proposed design is 76.4% the design met high degree of compactness and better efficiency.**

Keywords*—QCA; 2 Dot 1 Electron QCA; Comparator; Coulomb's principle

I. Introduction

Expansion of cost-effective, efficient nanotechnologies is conducting owing to obtain the performance that is not attainable by CMOS technology due to its scaling limits like off-state leakage current, degrading switching activity, etc. Quantum-dot cellular automata (QCA) technology is one of the up-and-coming replacements to overcome the scaling limits of CMOS [1]-[3]. QCA provides efficient properties including high- speed nano-scale designs at terahertz frequency range, long lifetime small feature size, together with low power consumption, ultra-low power dissipation [4]-[6].

One of the recent variant of QCA is 2 Dot 1 Electron QCA which offer all the advantages of QCA technology over conventional CMOS technology together with benefits over the 4 Dot 2 Electron QCA structure. The most advantageous aspect of 2 Dot 1 Electron QCA over 4 Dot 2 Electron QCA is the total number electron in the cell is halved, so energy requirement is reduced. There exits four ambiguous configurations in 4 Dot 2 Electron QCA, only two of them are valid. However, there is no ambiguous configuration in case of 2 Dot 1 Electron QCA [7]-[9]. Moreover in 2 Dot 1 Electron QCA wiring complexity is minimized as binary information can be transmitted from one cell to another using cell-to-cell interaction and obeying Coulomb's repulsion principle.

Comparator is fundamental digital devices and essential component for modern computing environments. There are diverse form of existing literature on comparator design using 4 Dot 2 Electron QCA as in [10]–[15]. Comparator design using 2 Dot 1 Electron QCA is unexplored till now. This article proposes an optimized comparator implemented using 2 Dot 1 Electron QCA cell.

The later part of the study is structured in the following way. Section II represents the overview of 2 Dot 1 Electron QCA. Section III offers design and scheme of a novel XOR gate. The design of proposed 1 bit comparators using the novel XOR gate is presented in section IV. Section V verifies the output energy states using standard mathematical procedure. Effective area analysis of the proposed architecture is provided in section VI. In section VII energy and power dissipation to run the proposed design is briefly analyzed. Finally Conclusion is demonstrated in section VIII.

II. Overview of 2 Dot 1 Electron QCA

The building block of Quantum dot Cellular Automata are cells and quantum dots or holes. Different formations of cells lead to different variants of QCA. Two dimensional 2 Dot 1 Electron QCA is the structural variation of QCA. As the name clearly suggests that a 2-Dot 1-Electron QCA cell consists of two logically interacting quantum dots and one electron. Single electron can move between the two quantum dots through the tunnel. Also, the single electron in the cell is able to represent binary information by the occupancy of electron in the quantum dots.

The cell structure of 2 Dot 1 Electron QCA is rectangular, either vertically or horizontally oriented along with two dots are at the two ends [9]. The structure of the 2-dot 1-electron QCA cells and their polarities are shown in Fig. 1(a) and 1(b). The position of the electron within a cell represents binary information.

In case of vertical cell when the electron positioned in the quantum dot below, and above, represent binary '0' and '1' respectively shown in Fig. 1(a) and 1(b). In the same way, in horizontal cell when the electron positioned in the right and left quantum dot represent binary '0' and '1' respectively.

However, like 4 Dot 2 Electron QCA 2 Dot 1 Electron QCA has fundamental design constructs such as binary wire, inverter by oppositely positioned cell between two same oriented cell of a binary wire, planar crossing of wires [7],

inverter by placing cell at corner and majority voter gate as depicted in Fig. 1 (c), 1 (d), 1(e), 1(f) and 2 respectively.

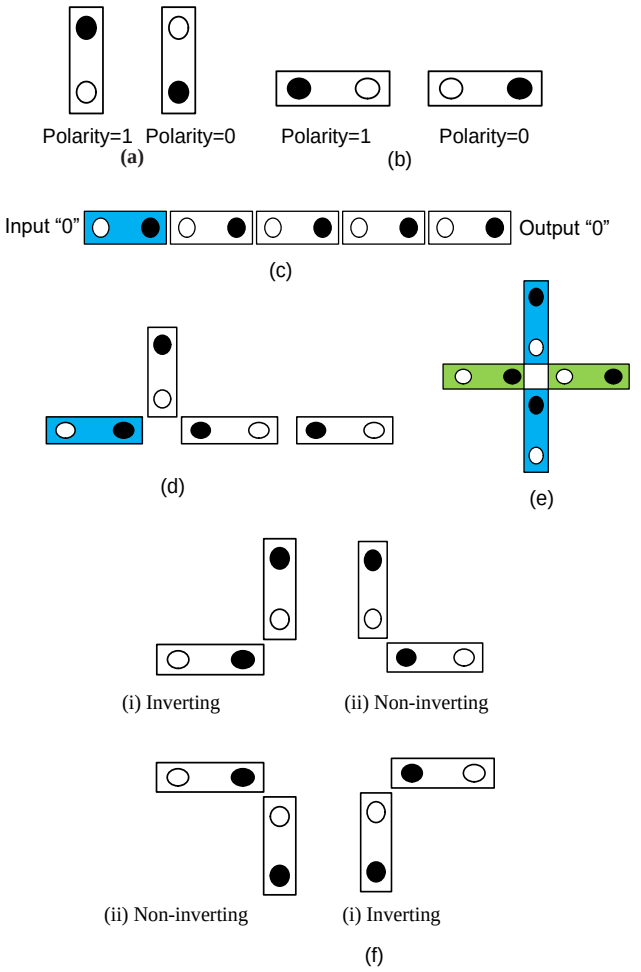

Fig. 1. The 2 Dot 1 Electron based(a) vertically aligned cells (b) horizontally aligned cells (c) binary wire (d) inverter (e) planar crossing of wires

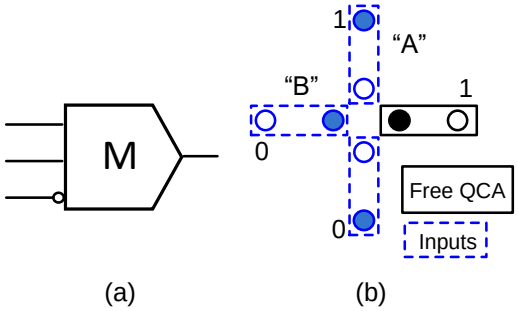

Fig. 2. Majority Voter (MV) gate (a) logical diagram and (b) 2 Dot 1 Electron QCA implementation

A. QCA Clocking

In CMOS technology clocking is used for the purpose of synchronization, whereas; in 2 Dot 1 Electron QCA architecture clocking fulfill two purposes. One is to control direction of data flow and other is to empower the weak input signals since they can traverse the whole circuit [8]. QCA clocking consists of four phases namely switch, hold, release, and relax.

One clock zone is out of phase with the subsequent clock zone by $\pi/2$ as depicted in Fig. 3(a) and several color codes indicate various clock zone as shown in Fig. 3(b).

In switch phase, initially electrons into the quantum dots contain minimum energy. The input signals are not adequate enough to empower the electrons. After that clock signal amplitude increases and potential energy of electrons begin to rise. Finally electron gains highest potential energy at the end of this phase.

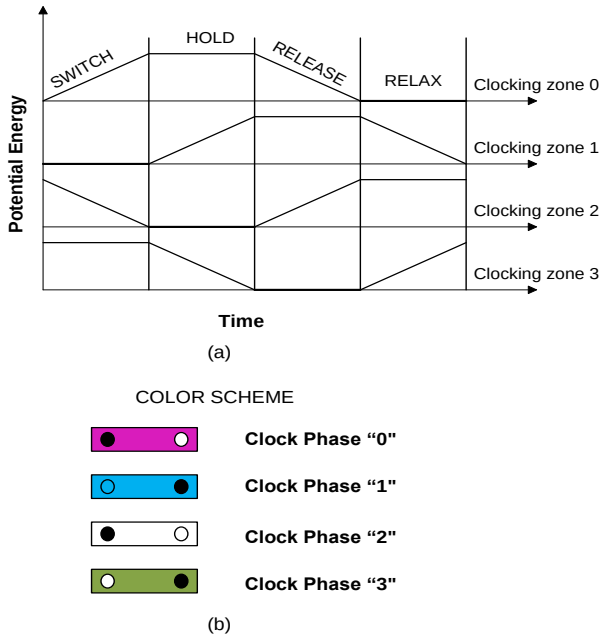

Fig. 3. (a) The 2 Dot 1 Electron clocking (b) color scheme of various clock zones

During the hold phase, the high phase, electrons become effectively energized to exceed the tunneling barrier. At this phase electrons loose polarity and get completely delocalized. The cells are stated to obtain null phase.

In the release phase, the high to low phase, actual computation is performed and electrons start to dissipate potential energy. They latch at the other quantum dots. The cells gradually begin to obtain a certain polarity.

In the relax phase, the low phase, electrons bear minimum energy and confined into the quantum dots. The cells in one clock zone will perform as input for the next clock zone.

III. The Novel Ex-Or Gate

A several form of XOR (exclusive-OR) gate has been designed until now [16], [17] and most of the cases utilized 3-input majority gate. In digital logic circuit designs XOR gate is an exigent element. Different XOR-based circuits have been designed yet, owing to the great essentiality of XOR gate [18]. Fig.4 illustrates the 2 Dot 1 Electron two input XOR Gate. However, the novel 2 Dot 1 Electron two input XOR Gate is not majority based rather it utilizes explicit interactions among QCA cells to determine the expected output.

IV. Proposed Design of 1 Bit Comparator

1 bit comparator as the name indicates that this digital logic circuit could be utilized to compare whether two 1 bit binary numbers are identical. Moreover it also identifies which number is larger. Therefore in logic circuits design 1 bit comparators are used for decision making. Fig.5 illustrates the schematic of 1-Bit Comparator using logic gates. Table I demonstrates the truth table of 1 Bit Comparator.

$$Y_{A>B} = A.\bar{B}$$
$$Y_{A<B} = \bar{A}.B$$
$$Y_{A=B} = \bar{A}.\bar{B}+A.B$$
$$= A \text{ XNOR } B$$

The proposed 1 bit Comparator has been implemented utilizing 2 Dot 1 Electron QCA. The design forms of two AND gates and one novel Ex-OR gate to determine the logic functionality of the 1 bit Comparator. In the proposed design there are two input A and B and three output A>B, A<B, A=B. the implementation of proposed 1 bit Comparator using 2 Dot 1 Electron QCA cell is depicted in Fig. 6.

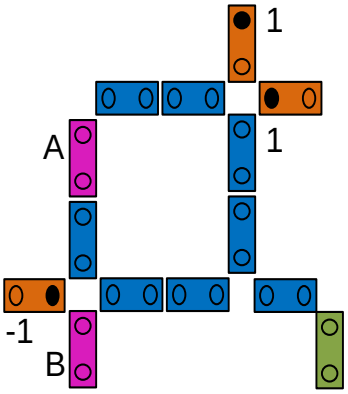

Fig. 4. (a) The 2 Dot 1 Electron two input XOR Gate

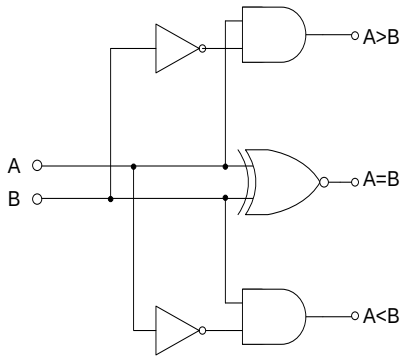

Fig. 5. Schematic of 1- Bit comparator using logic gate

TABLE. I. Truth Table of 1 Bit Comparator

Input		Output		
A	B	$Y_{A=B}$	$Y_{A<B}$	$Y_{A>B}$
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

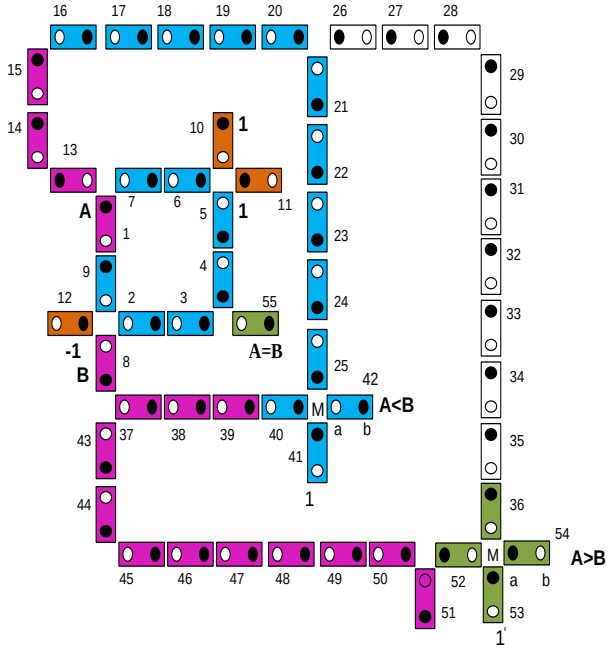

Fig. 6. 1 Bit comparator implemented using 2 Dot 1 Electron QCA cell

V. Estimation of Output Energy State of the Proposed Architecture

Since there is no available open source simulation software to simulate 2 Dot 1 Electron QCA circuit till now, like QCADesigner [19] for 4 Dot 2 Electron QCA architectures. Thus, this work utilizes a well-accepted standard mathematical function based on Coulomb's law to justify the proposed designs as available in [7] - [9], [20].

The calculation of potential energy between two electron charges is done using the following equations.

$$U = Kq_1q_2/r$$
$$Kq_1q_2 = 9 \times 10^{-9}(1.6)^2 \times 10^{-20}$$
$$U_T = \sum_{t=1}^{n} U_t \text{ .....(1)}$$

Where U indicates the potential energy between the two electron charges $q1$ and $q2$, K is the Boltzman constant and r denotes the distance between the two point electric charges. U_T denotes the total potential energy for a specific electron position because of the effects of all of its neighbor electrons. Electron and quantum dot contains negative charge and induced positive charge respectively. Electron, due to its characteristics always tends to reach at a position with least potential energy. Thus, to evaluate the output state of the proposed design, comparative analysis of the total potential energy is calculated for each of the allowable electron positions within a cell. Let, each of 2 Dot 1 Electron QCA cell has length = 13 nm and the space between two cell = 5 nm. Fig.6 represents the numbering of cell of the proposed comparator design using 2 Dot 1 electrons QCA and Table II presents respective potential energy evaluations.

VI. Effective Area Analysis

As mention before the structure of 2 Dot 1 electron QCA cells are rectangular. Consider the length and breadth of a 2 Dot 1 electron QCA cell is p and q respectively. Therefore area

of each cell is p×q nm^2. To form the proposed 1 bit Comparator 55 number of 2 Dot 1 electron QCA cell is required as shown in Fig. 6 Thus the effective area under the architecture is 55pq and the area covered by the architecture is 72pq. The ratio of area utilization of the proposed architecture is 55:72. The compactness is 76.4%. Hence the design met high degree of compactness.

VII. Energy and Power Dissipation Analysis

Various expressions are used as in [22], [23] to calculate energy parameters. E_m is the minimum energy to be provided to the scheme with *N* cells; E_{clock} is the energy applied by the clock to the circuit with *N* cells; E_{diss} is dissipation of energy from the circuit with *N* cells; $\boldsymbol{v}_2$ denotes frequency of energy dissipation; τ_2 is the time to dissipate to arrive to the relaxed state into the environment; $\boldsymbol{v}_1$ is the frequency of incident energy; τ_1 is the time needed to arrive from quantum level n_2 to the quantum level n. τ is the required time by the cells to switch from one to the subsequence polarization in a particular clock zone; t_p is propagation time to the entire circuit; $\boldsymbol{v}_1$-$\boldsymbol{v}_2$ indicates differential frequency. All of these parameter values for proposed 1 bit comparator are determined in Table III.

TABLE. II. Output State of 2-Dot I-Electron QCA Comparator

Cell	Position of electron	Cumulative potential energy	Comments
1, 8			Input cell A and B respectively
10, 12			Cell 10, 11 has fixed polarity "1".
11			Cell 11 has fixed polarity "-1".
4 – 7			Attain polarity from cell 10, 11 and A.
9			Gains polarity from input cell A
2, 3			Gain polarity from 8, 9 and 12.
55			Attains polarity from 3, 4.
37 – 40			Gain same polarity of input cell B.
13 – 15			Gain same polarity of input cell A.
16 – 25			Attain the inverse polarity of cell 15 (Fig.1(f) (iv))
41			Cell 41 has fixed polarity "1".
53			Cell 53 has fixed polarity "1".
37 – 40			Gain same polarity of input cell B.
42	a b	13.564×10−20 J 1.368 × 10−20 J	Electron will latch at position b due to less energy
26 – 36			Attains the inverse polarity of cell 21 (Fig.1 (f) (iv))
43 – 51			Gain same polarity of input cell B.
52			Attains the inverse polarity of cell 51 (Fig.1 (f) (iv))
54	a b	−3.329 × 10−20 J −0.537 × 10−20 J	Electron will latch at position a due to less energy

TABLE. III. Several Energy Parameter Values for Proposed 1 Bit Comparator

Parameters	Values
$E_{clock} = \frac{n^2\pi^2\hbar^2 N}{ma^2}$	3.9207×10^{-18} Joules
$E_{diss} = \frac{\pi^2\hbar^2}{ma^2}(n^2-1)N$	3.8815×10^{-18} Joules
$v_1 = \frac{\pi\hbar}{2ma^2}(n^2-n_2^2)N$	2.8407×10^{15} Hz
$v_2 = \frac{\pi\hbar}{2ma^2}(n^2-1)N$	2.92945×10^{15} Hz
$(v_1 - v_2) = \frac{\pi\hbar}{ma^2}(n^2-1)N$	8.875×10^{13} Hz
$\tau_1 = \frac{1}{v_1} = \frac{2ma^2}{\pi\hbar(n^2-n_2^2)N}$	3.5202×10^{-16} sec
$\tau_2 = \frac{1}{v_2} = \frac{2ma^2}{\pi\hbar(n^2-1)N}$	3.41361×10^{-16} sec
$\tau = \tau_1 + \tau_2$	6.93381×10^{-16} sec
$t_p = \tau + (k-1)\tau_2$	17.17464×10^{-16} sec

VIII. Conclusion

This present scope proposes an improved design methodology of 1 bit comparator using 2 Dot 1 Electron QCA which attains high degree of compactness and require lesser amount of energy to run. Since there is no open source simulation tool existing for 2 Dot 1 Electron. Therefore, potential energy calculation is applied in order to justify the proposed design. In addition effective area and stability is presented to analyze the acceptance level of the architecture. Several energy parameters and power dissipation are also analyzed for the proposed scheme.

References

[1] Lent, C. S., Tougaw, P. D., Porod, W., & Bernstein, G. H. (1993). Quantum cellular automata. *Nanotechnology*, *4*(1), 49.

[2] Liu, W., Lu, L., O'Neill, M., & Swartzlander, E. E. (2011, May). Design rules for quantum-dot cellular automata. In Circuits and Systems (ISCAS), 2011 IEEE International Symposium on (pp. 2361-2364). IEEE.

[3] Kim, K., Wu, K., & Karri, R. (2005, March). Towards designing robust QCA architectures in the presence of sneak noise paths. In Proceedings of the conference on Design, Automation and Test in Europe-Volume 2 (pp. 1214-1219). IEEE Computer Society.

[4] Bahar, A. N., Rahman, M. M., Nahid, N. M., & Hassan, M. K. (2017). Energy dissipation dataset for reversible logic gates in quantum dot-cellular automata. Data in Brief, 10, 557-560.

[5] Abdullah-Al-Shafi, M., & Bahar, A. N. (2016). Novel binary to gray code converters in QCA with power dissipation analysis. International Journal of Multimedia and Ubiquitous Engineering, 11(8), 379-396.

[6] Sheikhfaal, S., Angizi, S., Sarmadi, S., Moaiyeri, M. H., & Sayedsalehi, S. (2015). Designing efficient QCA logical circuits with power dissipation analysis. Microelectronics Journal, 46(6), 462-471.

[7] Ghosh, M., Mukhopadhyay, D., & Dutta, P. (2015). A 2 dot 1 electron quantum cellular automata based parallel memory. In Information systems design and intelligent applications (pp. 627-636). Springer India.

[8] Hook IV, L. R., & Lee, S. C. (2011). Design and simulation of 2-D 2-dot quantum-dot cellular automata logic. IEEE Transactions on Nanotechnology, 10(5), 996-1003.

[9] Ghosh, M., Mukhopadhyay, D., & Dutta, P. (2016). 2-Dimensional 2-Dot 1-Electron Quantum Cellular Automata-Based Dynamic Memory Design. In Proceedings of the 4th International Conference on Frontiers in Intelligent Computing: Theory and Applications (FICTA) 2015 (pp. 357-365). Springer India.

[10] Mukhopadhyay, D., Dinda, S., & Dutta, P. (2011). Designing and implementation of quantum cellular automata 2: 1 multiplexer circuit. International Journal of Computer Applications, 25(1), 21-24.

[11] Ke-ming, Q., & Yin-shui, X. (2007, October). Quantum-dots cellular automata comparator. In ASIC, 2007. ASICON'07. 7th International Conference on (pp. 1297-1300). IEEE.

[12] Lampreht, B., Stepancic, L., Vizec, I., Zankar, B., Mraz, M., Bajec, I. L., & Pecar, P. (2008, September). Quantum-dot cellular automata serial comparator. In Digital System Design Architectures, Methods and Tools, 2008. DSD'08. 11th EUROMICRO Conference on (pp. 447-452). IEEE.

[13] Wagh, M. D., Sun, Y., & Annampedu, V. (2008, June). Implementation of comparison function using quantum-dot cellular automata. In Proc. Nanotechnol. Conf. Trade Show (pp. 76-79).

[14] Xia, Y., & Qiu, K. (2009). Comparator design based on quantum-dot cellular automata. J. Electron. Inf. Technol, 31(6), 1517-1520.

[15] Abdullah-Al-Shafi, M., & Bahar, A. N. (2016). Optimized design and performance analysis of novel comparator and full adder in nanoscale. Cogent Engineering, 3(1), 1237864.

[16] Bahar, A. N., Uddin, M. S., Abdullah-Al-Shafi, M., Bhuiyan, M. M. R., & Ahmed, K. (2017). Designing efficient QCA even parity generator circuits with power dissipation analysis. Alexandria Engineering Journal.

[17] Bahar, A. N., Waheed, S., Hossain, N., & Asaduzzaman, M. (2017). A novel 3-input XOR function implementation in quantum dot-cellular automata with energy dissipation analysis. Alexandria Engineering Journal.

[18] Bahar, A. N., Waheed, S., & Hossain, N. (2015). A new approach of presenting reversible logic gate in nanoscale. SpringerPlus, 4(1), 153.

[19] Walus, K., Dysart, T. J., Jullien, G. A., & Budiman, R. A. (2004). QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE transactions on nanotechnology, 3(1), 26-31.

[20] Bahar, A. N., & Waheed, S. (2016). Design and implementation of an efficient single layer five input majority voter gate in quantum-dot cellular automata. SpringerPlus, 5(1), 636.

[21] Hashemi, S., Farazkish, R., & Navi, K. (2013). New quantum dot cellular automata cell arrangements. Journal of Computational and Theoretical Nanoscience, 10(4), 798-809.

[22] Mukhopadhyay, D., & Dutta, P. (2015). A study on energy optimized 4 dot 2 electron two dimensional quantum dot cellular automata logical reversible flip-flops. Microelectronics Journal, 46(6), 519-530.

[23] Angizi, S., Alkaldy, E., Bagherzadeh, N., & Navi, K. (2014). Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. Journal of Low Power Electronics, 10(2), 259-271.