Low Error Floor Concatenated LDPC for MIMO Systems

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***Abstract*—Multiple-Input and Multiple-Output, or MIMO is the use of multiple antennas at both the transmitter and receiver to improve communication performance. MIMO technology has attracted attention in wireless communications; because it offers significant increases in data throughput and spectral efficiency without additional bandwidth or increased transmit power. To achieve the mentioned above performance Bit Error Rates (BER) should be low. For this reason efficient encoding and decoding algorithms should be used. MIMO systems rely on error-control coding to ensure reliable communication in the presence of noise. Forward Error Correction Codes (FEC) such as convolutional and block codes were investigated for MIMO systems. Low Density Parity Check (LDPC) shows good performance except that an error floor may appear at high Signal to Noise Ratio (SNR). In this work we propose a concatenated error control code that reduces the error floor of LDPC codes suffering from error floor. The proposed scheme is a good candidate for high rates real time communication since it reduces the decoding latency as well.**

Keywords—LDPC; error floor; MIMO; error control

I. INTRODUCTION

One important issue with wireless communication systems is providing high data rates. MIMO systems provide high channel capacity and so may provide high throughputs which are promising for 4G and 5G. However, high data throughputs are conditioned with low bit error rates. Error control codes are deployed to decrease BER and so increase channel throughputs. In the literature, both convolutional codes (CC) and block codes were investigated for MIMO systems. CC and LDPC codes were improved in many types of research by serial and parallel concatenation. CC gained interest because of their decoding process based on the Viterbi decoder [1]. They attracted more attention because of their use in Turbo codes. Turbo codes were first proposed by Berrou in [2] where the authors proved that turbo codes may attain near Shannon capacity performance.

One competitor of turbo codes is the linear block Low Density Parity Check (LDPC) [3], [4]. It was shown that the LDPC codes are good enough to achieve performance close to the channel capacity. Potentials of LDPC codes for MIMO system were revealed in many researches [5], [6] and [7]. In [8] , simulation results showed that LDPC outperforms turbo codes in both correlated and uncorrelated Rayleigh channels. In [9], they showed that LDPC decoding presents a lower complexity than turbo codes because of the ability to stop whenever a code word is reached. In addition, LDPC decoder could be implemented in parallel which improves its performance for long codes. Authors in [10], compared LDPC to CC with respect to decoding latency consideration. They showed that at low and intermediate latency, CC with Viterbi and stack sequential decoders outperform LDPC.

In this work, a concatenated code which improves both LDPC BER performance at high SNR and channel decoding latency is proposed. This paper is organized as following: In section II, a concatenation of three channel codes with LDPC as inner code is proposed. Afterward in section III, undertaken simulation results are provided revealing good performance of the concatenated scheme compared to a standalone LDPC channel code mainly in case of error floor presence. In section IV, a discussion of the found results is conducted.

II. LITERATURE REVIEW

LDPC codes suffer from error floors that appear at high SNRs [11]. Error floors could be reduced through post-processing or concatenation [12]. In [13], both CC and LDPC are improved by their serial concatenation. LDPC is used as an outer code and CC is used as an inner code. They showed that the LDPC-CC scheme improves both CC and LDPC codes mainly at high SNR. In [14], authors used an iterative detection decoding schema where both soft input soft output MMSE with successive interference cancellation and LDPC are processed iteratively. They showed that the iterative detection decoding scheme improves BER by a 2dB in a 2 by 2 MIMO system. Some studies focused on the design of the LDPC parity matrix to improve the later code performance. In [15], authors designed an irregular LDPC parity matrix; where weights of variable nodes and check nodes are variable. They showed that using appropriate irregular codes improves the BER performance. In [16], a BICM interleaver was used to reduce the error floor. In [17] a two-staged weighted bit flipping decoding algorithm was proposed. The proposed algorithm reduces the error floor although it has high complexity which remains lower than a simple bit flipping algorithm. In [18] , a Progressive Edge Growth algorithm which takes advantage from the LDPC graph structure is used at the decoder to improve the LDPC performance. In [19], authors proposed a method of lowering the error floor by intelligently inserting a pilot bits or known bits in the message frame. This provides high log-likelihood information which improves decoding output. In [20], Quantum LDPC codes construction decreases the error floor.

III. System Architecture

A concatenation of three channel codes is proposed; LDPC is the inner code, BCH is the outer one and CC is the mid one as given in Fig. 1 Serial concatenation of channel codes were first introduced by Forney [21]. This technique induces longer codes with better BER and lower decoding complexity. Generally, CC codes are serially concatenated to Reed Solomon (RS) codes [22]. RS is used as an outer code to correct the error bursts resulting from the CC Viterbi decoder.

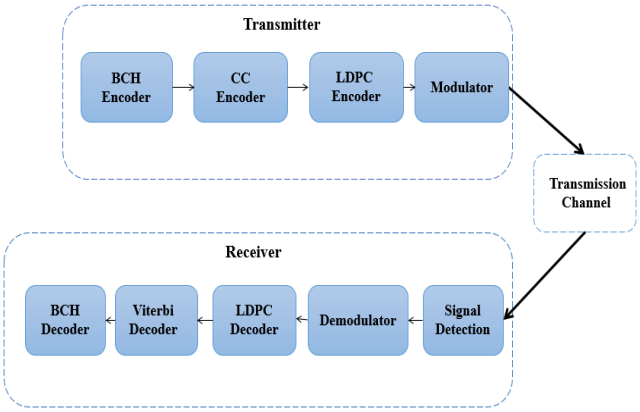

Fig. 1. Proposed Architecture

The received signal is estimated by a Vertical Bell Laboratories Layer Space-Time Minimum Mean Square Error (VBLAST-MMSE) based detector [23]. After the demodulator a belief propagation LDPC decoder is implemented followed by a soft decision Viterbi decoder and finally a BCH decoder. Viterbi decoder main flaw is the generation of burst of error which we mitigate through the use of BCH decoder.

A. Convolutional Codes [1]

In convolutional codes, the encoding process is based on the use of a generator polynomial implemented as a shift register. Convolutional codes are defined as $C(n, k, l)$ codes where n is number of output bits, k is the number of input bits and l is constraints length representing number of memory registers. The Trellis based structure of the convolutional codes make the Viterbi decoding suitable for them.

B. Low Density Parity Check Code

Low Density Parity Check codes were proposed by Gallager in 1962 [3]. They were first ignored for almost a decade then they regain interest. LDPC regains interest because of its linear structure and iterative decoding process. LDPC codes are represented by their parity check matrix. Each row in the parity check matrix represents a parity equation. The number of columns represents the code length. Regular LDPC codes are codes where the number of ones per rows is constant (row weight) and number of ones per columns are constant (column weight) [24]. Whereas irregular codes are the ones where number of ones per rows are not equal (row weight) and number of ones per columns are not equal (column weight). LDPC codes maybe represented by their parity matrix as in Eq.1:

$$H = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \end{bmatrix} \quad \text{Eq. 1}$$

LDPC codes are also represented by the bipartite Tanner Graph, Fig. 2. Tanner graph have two sets of nodes Check nodes and Variable nodes. Check nodes represent the rows of the parity check matrix. Variable nodes represent the columns of the matrix. Following is the Tanner graph of the parity matrix H.

Several regular and irregular parity check matrix construction methods were proposed in the literature. Indeed, Tanner graph structure and hence parity check matrix structure alter the code performance; girth length, trapping set size. Small girth leads to error floors with iterative decoding. Error floor is one main challenging problem of LDPC codes [25].

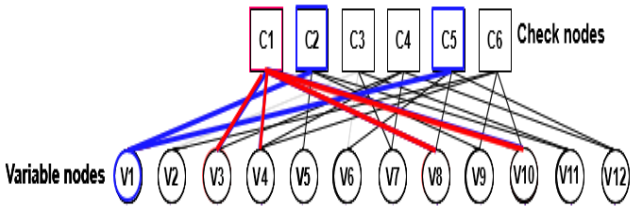

Fig. 2. LDPC Tanner Graph

Message passing decoding algorithm is used between nodes to correct errors. Message passing for hard decoding is implemented through bit flipping algorithm. On the other hand, soft decoding is implemented by the belief propagation (BP) algorithm. In BP likelihood information is exchanged between variable and check nodes. Check nodes and variable nodes keep exchanging the likelihood information until a null syndrome or a maximum number of iterations are reached [3]. Bit flipping algorithm attracts many researches because of its low complexity compared to BP even though it suffers from lower performance and higher error floor.

C. BCH Codes

The Bose, Chaudhuri, and Hocquenghem (BCH) codes form a large class of powerful random error-correcting cyclic codes. For any positive integers $m \geq 3$ and $t < 2^{m-1}$, there exists a binary BCH code with block length $n = 2m - 1$, number of parity-check digits $n - k \leq mt$ and minimum distance $dmin \geq 2t + 1$. We call this code a t-error-correcting BCH code. BCH code is chosen for this concatenated scheme for its flexibility in the sense that different coding rate codes are easily constructed. Actually, BCH is used instead of Reed Solomon for the simplicity of code construction for different coding rates and for its low encoding decoding complexities.

IV. Simulation Results

Simulations were conducted on the worst cases of LDPC codes; short, with small girth in a Rayleigh flat fading channel. Binary Phase Shift Key (BPSK) modulation with a VBLAST-MMSE detector is implemented. A (15, 11) BCH code and a [5, 7] code with ½ coding rate CC code with constraint length equal to 3 were considered. Simulations were conducted for both girth four and free of girth four LDPC codes. Also, a bit flipping decoding was considered for its low complexity and clear error floor.

In Fig. 3, Simulations were conducted for girth four LDPC parity check matrix. The ¼ LDPC-BCH-CC scheme is compared to a standalone ¼ LDPC code. The VBLAST-MMSE-concatenated code achieves better BER compared to the standalone LDPC code. Also, by comparing BER of the standalone LDPC for different MIMO systems it is noticed that receive antenna diversity improves LDPC BER performance and reduces the error floor. Obviously, the concatenated model reduces the error floor obtained in a 1 by 2 MIMO system. In addition, the coding gain of the concatenated scheme increases from 0.5dB in a 2 by 8 MIMO system to reach almost 1.5dB in a 1by 2 MIMO system at 10^{-2}. As stated previously authors in [13] proposed a concatenation of a 5/6 LDPC and ½ CC with CC as an inner code outperforms slightly a ½ LDPC code in a SUI-3 channel model.

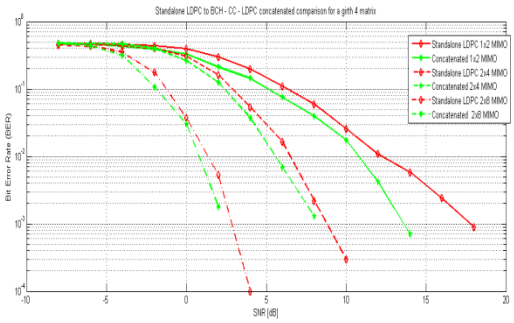

Fig. 3. Concatenated to standalone codes comparison for girth four LDPC matrix

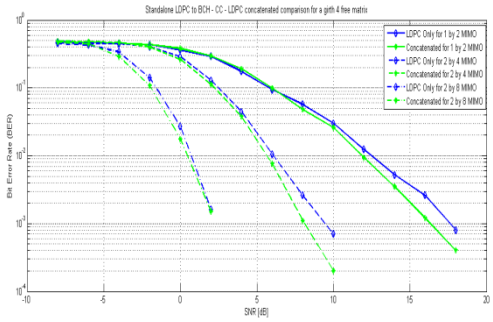

Fig. 4. Concatenated to standalone codes comparison for girth four free LDPC matrix

In Fig. 4, simulations were conducted for girth four free LDPC parity check matrix. The ½ coding rate LDPC code is the MacKay regular matrix 96.33.964 [4]. Notice that the coding gain increases when MIMO receive diversity decreases as in Fig. 3. Also, notice that the gain obtained for a girth four LDPC matrix is better than the gain obtained for a girth four free LDPC matrix.

V. Discussion

Simulation results showed that BCH, CC and LDPC concatenated code outperforms a standalone LDPC code which may suffer from error floors mainly when the parity check matrix has a girth equal to four. In fact, the CC decoder corrects errors remaining after the LDPC hard decoder. In addition to error floor reduction this concatenated scheme improves the decoding latency. In **[27]**, authors stated that the LDPC decoding latency equals the arrival time of one block plus the average computational time needed for decoding and buffering which depends on the number of iterations. Whereas the decoding latency of a convolutional code equals the arrival time of one incoming trellis (or tree) section (k*m information bits for an (n, k, m) convolutional code) plus the Viterbi decoder computation time which is a constant. So, when using a ½ LDPC decoder with CC and a short BCH code the decoding latency is reduced compared to a ¼ standalone LDPC. Also, the storage need of a Trellis decoder related to the constraint length is much lower than the buffer needs of an iterative block LDPC decoder. This raises the importance of using a BCH-CC-LDPC concatenated schema for real time communications for the next communication systems generations.

VI. Conclusion

Channel codes should provide high channel efficiency with small code rate, low decoding complexity and low BER. It was shown in the literature that LDPC codes outperforms both CC and turbo codes which were dominating just before LDPC. Main disadvantages of LDPC code are the appearance of an error floor at high SNR and the high decoding latency. In this work, a concatenation of BCH-CC-LDPC for MIMO system is proposed. A concatenation of a reduced LDPC code rate with a CC convolutional code and a BCH code instead of using one standalone LDPC reduces the error floor mainly in case of girth four LDPC matrix. Also, the concatenated scheme improves the performance of a low receive diversity MIMO system. Finally, the concatenated schema enhances the system decoding latency because an LDPC decoder is replaced by a CC decoder and a short BCH decoder which have lower decoding latencies than LDPC. The performance of the proposed system could also be enhanced in case of LDPC convolutional codes.

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