An Efficient Fault Tolerance Technique for Through-Silicon-Vias in 3-D ICs

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***Abstract*—Three-dimensional integrated circuits (3D-ICs) based on Through-Silicon-Vias (TSVs) interconnection technology appeared as a viable solution to overcome problems of cost, reliability, yield and stacking area. In order to be commercially feasible, the 3D-IC yield must be as high as possible, which requires a tested and reparable TSVs. To overpass this challenge, an integration of interconnect built-in self-test (IBIST) methodology for 3D-IC is given in the aims to test the defectives TSVs. Once the interconnection has been tested, the result extracted from IBIST initiate the repairing defectives TSVs based on the built-in self-repair (BISR) structure. This paper superposed two fault tolerance techniques in particularly the redundant TSV and the time division multiplexing access (TDMA) in case of multi defectives TSV. This novel repair architecture increase the yield of 3D-ICs in a high failure rate. It leads to 100% reparability for 30% failure rate. A parallel processing approach of the proposed structure is presented to accelerate the test and repair operations. Achieved experimental results with the proposed methodology scheme show a good performance in terms of repair rate and yield.**

***Keywords*—Fault tolerance; 3D-IC; TSV; IBIST; BISR; TDMA**

I. INTRODUCTION

The 3D-ICs with TSVs provides smaller interconnect delay and higher device density [1]. These characteristics allow for the fastest IC design that offers flexible and low-cost packaging solutions. Interconnection of the various tiers troughs the TSVs pledges to increase the interconnect bandwidth and the performance of 3D-ICs while lowering power dissipation and manufacturing cost [2], [3]. Nevertheless, there are several challenges that can affect and decrease 3D ICs yield, i.e., technological challenges, test challenges, thermal and power challenges and infrastructure challenges [4]. In other terms, to guarantee the quality of the 3D chips, the TSV must be tested to locate manufacturing defect, a lack of precision in every fabrication step or integration process can produce a several kind of defects as revealed in Fig. 1 [5].

All the kind of defect decrease the performance of TSVs channels in terms of electrical characteristics and reduces the ability to withstand physical and thermal stresses during and after the fabrication process [6], [7]. The defect mechanisms must be deeply assessed to decrease the failure in terminal product. Thus, a test of TSVs is very challenging because current wafer-level testing cannot deal with a large number of small TSVs at an affordable cost. Hence, an IBIST technique with low hardware overhead becomes a potentially good solution to achieve both test and cost-effectiveness [8].

Testing and repairing the 3D-ICs was considered as a key challenge to improve yield and reliability [9]. In the last few years, several researchers on 3D IC testing and TSVs repairing have been proposed [9]–[20]. The plurality of proposed solution in the literature to repair defective TSV based on adding redundant TSVs method by several design technique [9]–[15]. However, the redundant TSV made to repair one faulty [10]. One spare TSV for each defectives TSVs must been used in the repair process.

From area distribution and performance enhancement, it can be concluded that is not practicable to fabricate a redundant TSV for each one. Thus, the adopted technique to minimize number of spars TSVs was implemented to divide TSVs into sets with redundant TSV. After test process was achieved, a spares is used by shift operations [11], [12], to replace faulty TSVs. In [11] and [16] a novel amelioration of repairing methodology was proposed. It enables to exchange faulty TSVs by distant redundant TSVs. In [20] a new fault-tolerant technique was addressed without using of redundant TSV. The basic idea is to localize defective TSVs and rerouting the signal through faulty free one using time division multiplexing access (TDMA) technique. Although this evaluations in repairing.

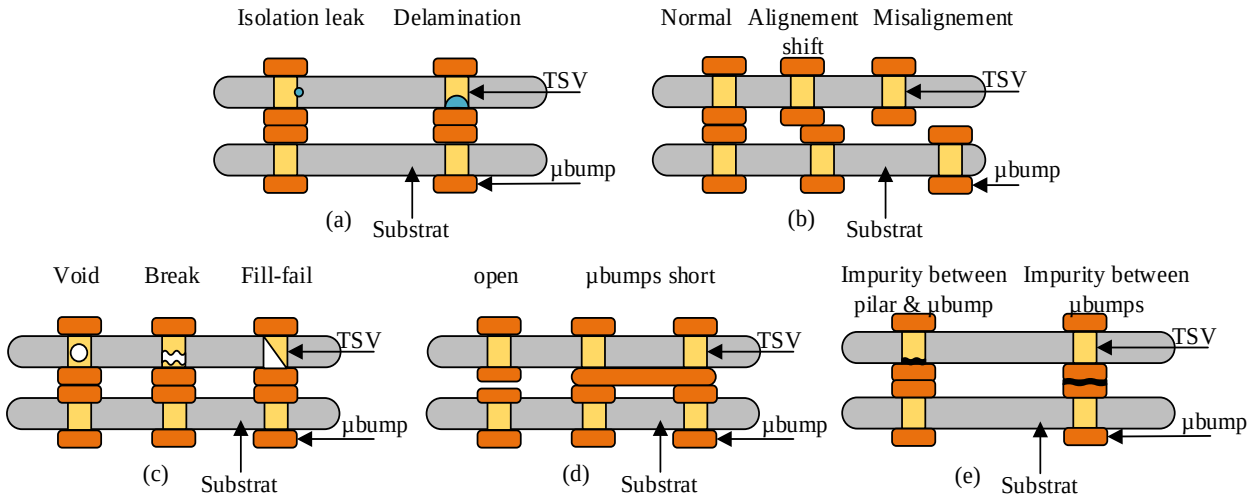


Fig. 1. Schematic presentations of TSV defects: (a) Defects due to substrate; (b) Defects due to misalignment; (c) Defects due to Cu pillar; (d) Defects in micro-bump; (e) Defects due to impurities.

This paper proposes a novel test and repair methodology of TSVs defect in 3D-ICs that integrates IBIST and BISR techniques. The proposed TSV's test architecture use the IBIST methodology in which a parallel test is applied in dies (layer) to speed the test process. The outcomes of the test results are investigated with a view to repair the identified faulty TSVs. The classification of TSVs into clusters with spare TSV aims to increase reparability rate. This work extends the repairing capabilities of BISR by enabling the correction of multi defectives TSVs based on TDMA technique. In fact, the TSV cluster was portioned in two bundles in which the shifting and replace process were properly implemented to transmit data. Moreover, the data is sequentially conveyed in two packets based on TDMA technique, which increase the number of spare TSV in each cluster.

The remains of this paper are organized as follows. Section II demonstrates the proposed combination between the new IBIST structure and the repairing architecture BISR. Section III presents the proposed repair process. Experimental results are illustrated in Section IV. Finally, conclusions are drawn in SectionV.

II. Proposed 3D IC based IBIST Methodology Test with TSV Repair

A. Testing TSV based IBIST Methodology

Fig. 2 presents the IBIST architecture, which is composed of detecting circuit, which is designed to be included between, transmitter and receiver components of each layer. The controller manages the different test tasks by means of an appropriate algorithm. The main component to detect the defectives TSVs is the test pattern generator (TPG) that includes a linear feedback shift register (LFSR).

The pattern source generates the test vectors, which are employed to test the TSVs. It comprises a sub-circuit that provides the LFSR functionality [18]. LFSR is a shift register used to generate pseudo-random test vectors. In the proposed test architecture, pattern generator in layer k-1 sends a test vector to layer k to test a k group of TSV in order to accelerate the test process for a big number of TSV groups. The test vectors are generated at layer k are simultaneously sent to the layer k+1 and the XOR logic port. In which the pattern coming from the layer k-1 is analyzed with XOR gate.

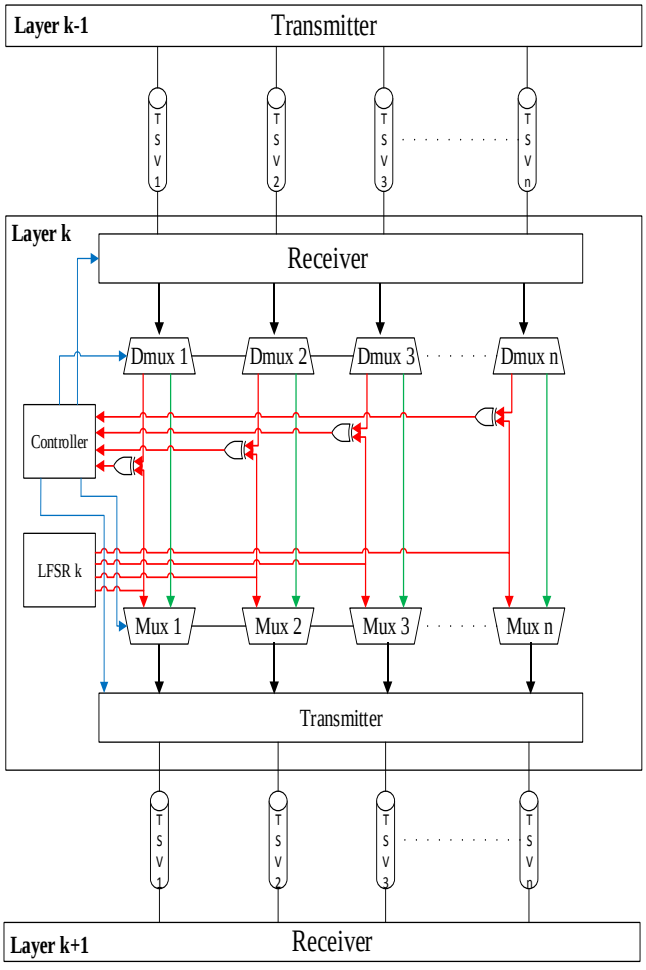


Fig. 2. The proposed architecture of the IBIST technique.

When the IBIST is in the test mode, the test vectors will be transmitted to the TSVs under test. In the end of test process, the test result well introduce to the analyzer. This last gives out an error signature, based on comparison between test data resaved from layer k-1 and data generated in layer k, which localize the defectives TSVs. This last step in test process verified the state of TSV, whether is correct or has another impact. While the analyzer is composed of XOR gate, according to the error signature (0, means that the TSV under test is defect free) or (1, means that the TSV is defective).

The controller in Fig. 2 is the management of the data traffic and getting synchronization between several blocks of circuits. It starts by producing a test pattern with LFSR bloc and continue the computation path by triggering the generated pattern from the layer k-1 to layer *k* via TSVs groups. Thereafter, the received test pattern at layer k will be analyzed according to same vectors generated in this last. Thus, the faulty TSVs are labeled and localized. Then, the result given by the analyzer stocked in the signature register. Moreover, the controller's backup register can be used to reduce the allocated area of BISR and IBIST .The algorithm controlling the IBIST process test procedure in all 3D-IC rows. The labeled localized signal information will be transmitted to the BISR component to start repair step.

B. Architecture for TSV Repair

To enhance the yield of TSVs, it is crucial to extend the test architecture shown in Fig. 2 to support the TSV repair step. Fig. 3 shows the conceptual scheme of the enhanced repair TSV architecture. The repair circuits are inserted at the two terminals the transmitter and the receiver. In addition, a repair register designed in the bottom die for storing the repair information (error signature and selected signal of MUXs) of all dies (each die have a repair register to store repair information of TSV between dies). Each terminal of a TSV has one MUX to switch the signal path of TSV and exchange defective ones by redundant TSV.

The error signature is extracted from IBIST component to the repair register in first step of repair process. In this architecture, a spare TSVs (STSV) is used to repair in case of one defective TSV. The MUXs is serves to switch signals that give more flexibility in the substitution of the faulty TSV and repair the crosstalk noise. Crosstalk defect is the most widely mentioned hindrance of 3-D. It emerges due to undesirable interaction between TSVs and active components like the MOSFET and the FinFET or among TSVs [21].

In the second step of repair process, two classes are proposed based on the number of defectives TSVs. The premier one is launched at the detection of unique defective TSV as illustrated in Fig. 4(a). The defective TSV is insulated and switched by redundant TSV. Fig. 4(b) and (c) describe the second-class, which start in case of detecting multi defectives TSVs based on TDMA fault tolerance technique.

In [22] a high-speed time division multiplexing (HSTDM) methodology was instituted to bridge problem of high frequency of traffic in FPGA communication while not altering the delay. Furthermore, according to this new added HSTDM technique, no additional delay was acquired with strict time budgeting and user-constraints [22]. The introducing of the TDM technique in the aim to reduce the complexity of the global interconnect hardware and to reduce the global area and power consumption, lead to the efficiency very high inter-FPGA communication. The range of transferring data on the TSVs at very high clock frequency is in the scale of Giga hertz [23]. By this ability to transmit data in high-frequency TSV used as high-speed interconnects in [24] and they are served as inter-die communication interface in 3-D NoC [25].

Therefore, the high-speed characteristics of TSV can be exploited to design TDMA-based 3-D IC. The high-data-rate transfer were achieved by the design operating at high clock frequency for inter-die communication this lead to no extra delay is induced on signal path.

The principal idea in repair using TDMA technique is to subdivide input bits in tow bundle. The first faulty TSV is switched by using the spare then the three bits of available TSVs is shipped from bottom to upper layer and stored in a FIFO.

After that the bit of second defective TSVs are transmitted on fault-free ones (Fig. 4(c)). If all bits are correctly saved in FIFO, then it will be triggered to the output. Input data bits are organized in two bundles in the case of multi defectives TSVs that lead to increase the number of spare TSVs for each bundle. For example, in Fig. 4(b) there are four TSVs and one spare.

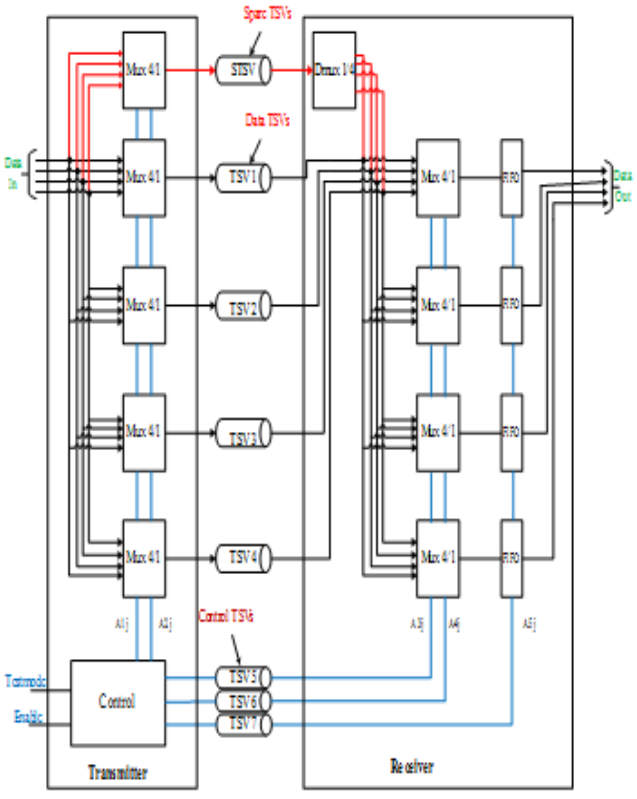


Fig. 3. Built-in Self-Repair (BISR) architecture for TSV defect.

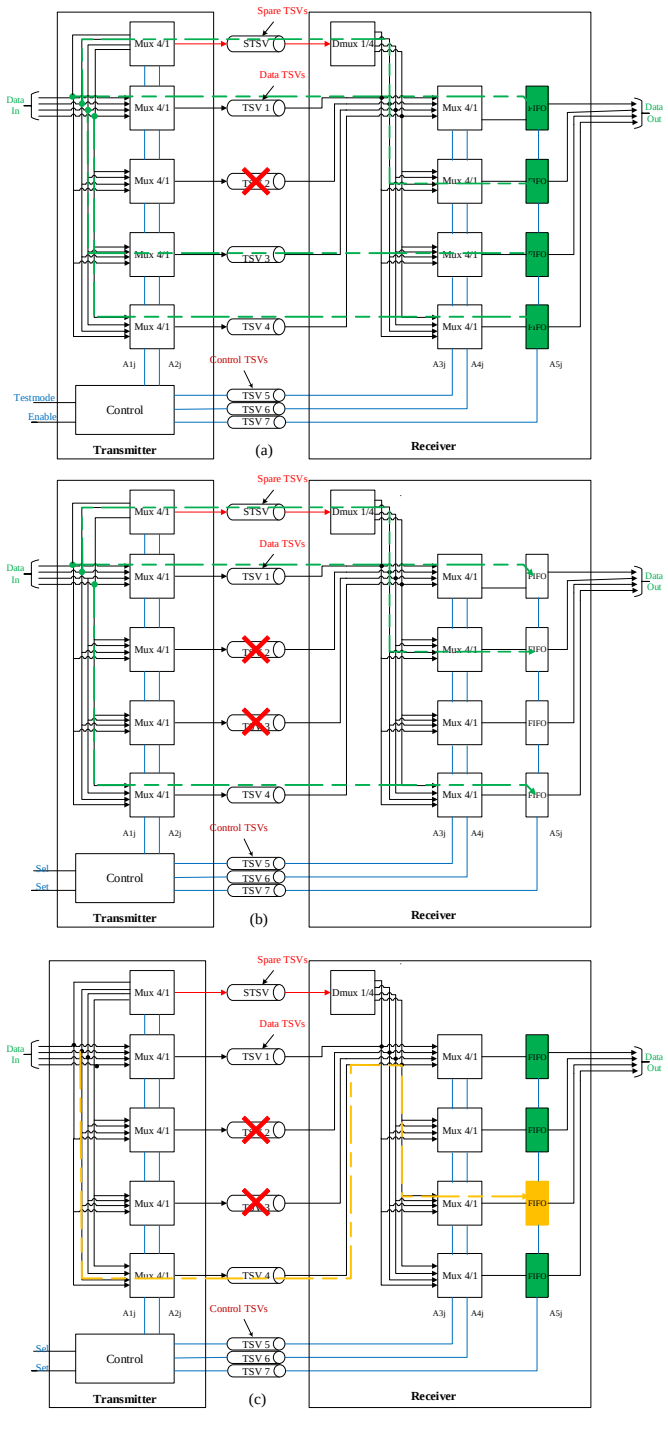


Fig. 4. Type of repair process: (a) Repair in case of one faulty TSV; (b)-(c) Steps of repair process in case of defectives TSVs.

Spare TSVs for each bundle. For example, in Fig. 4(b) there are four TSVs and one spare. In state of two defectives TSVs, TDMA is exploited and then the first bundle that comprise three bits are send on the two fault-free and spare TSVs in the repair process (Fig. 5). In Fig. 4(c), three TSVs are valid to send the last bit, as three spare instead of one (i.e. the other available TSV are counted as spares).

Algorithm proposed test and repair technique

Algorithm proposed test and repair technique
Input: Number of regular TSV 'N'
Output: IBIST and BISR, Testing and repairing modules

1 Grouping of regular TSV with 'n' TSV per group plus spare TSV
2 Building of IBIST and BISR, testing and repairing modules
% Testing of TSVs for fault detection
3 While testmode= 1 do
4 for I=1 to n do
5 Generate test vectors and test TSV
% Transmit test vectors from die1 to die2 through TSVs
6 Analyze test vectors in die2
7 Testresult is passed to the repairing modules
% Re-routing of signal through defective-free TSVs
8 If (testresult=1)
9 Cut-off the signaling path of defective TSV
10 Switching the signal by spare TSV
11 If (multidefect=1)
12 Re-route the signal based on TDMA
13 end if
14 end if
15 end for
16 end while
% Normal mode of operation
17 If (testmode= 0 and testresult=0) // Normal mode
18 Pass input signals from die1 to output signals on die2
19 end if
20 Return proposed test and repair technique

Fig. 5. Algorithm of the proposed test and repair technique.

C. Enhanced Test Architecture for TSV Repair

A new test structure proposed for the TSV repair in the aim to reduce the area distribution and the cost. As described in previous section, to stock the control signals of repair architecture a new repair register is needed. The reconfigurable architecture has a new register for each TSV. As Fig. 3 shows, repair register aims to control the switching of repair MUXs. This proposition is to get the control signals of repair MUXs in the test process by overall enable signal (A_{ij}).

Fig. 6 presents a normal test operation of 3D-IC after repairing component receives error signature. In this simulation, When error signature (error in Fig. 6) is "0000000" that means there isn't a defect in the TSVs that leads to the normal operation. Then data_OUT receives data_IN without passing in repair component.

The new enunciated TSV self-repair architecture is auto performed in chip, based on the error signature delivering by IBIST, which identifies faulty TSVs. The BISR include a control, match register/MUXs, TSV mapping unit and TSV spared. When the control in BISR receives the trigger signal or address of faulty TSVs from IBIST, the repair process will be started immediately. After match register/MUX receives the labeled localized information from signature register via a controller in IBIST, the information should be decoded at first to acquire the reallocation of defective TSVs.

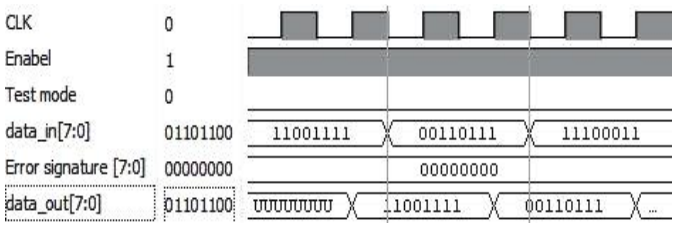


Fig. 6. Simulation of IBISR architecture in normal operation.

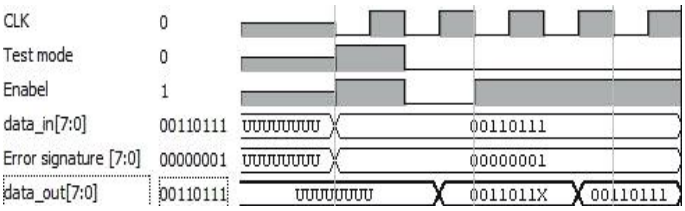


Fig. 7. Simulation of IBISR architecture in repairing operation.

TSV mapping unit will repair the defective TSVs by the method of shifting and replacing as shown in Fig. 7 that presents the simulation results of the repairing method. If there is any defective TSV, the MUX will isolate the defective TSV by labeled positional information, and switch the signal to the neighboring TSV. In Fig. 7, the test pattern is sent in 8 bits from layer1 to layer 2 of 3D-IC to test TSVs. After analyzing data in layer 2 data test, error signature stored in repair register and it used to repair TSV. In this simulation, there is "00000001", the bit in high-level indicates the defect location. For instance, the BISR uses the first type of repair process; the signal through the defective TSV originally will be switched to the neighboring TSV. The count of STSVs (spare TSVs) has an effect on the performance of the overall BISR scheme and increases the reparability in the proposed architecture. Moreover, the yield of 3D IC will be positively influenced. Using the parallel processing of IBIST and BISR will reduce the processing time of BISR structure.

To compare the proposed repair architecture of TSV and those of existing methodology, the difference is in using the multiplexer (MUX) for repairing. In fact, the MUX increases the number of register and signal in the circuit but it has a good advantage. Moreover, the use of the coder makes the solution more flexible to move the defective TSV to another TSV and overcome all problem like the crosstalk defect.

III. Experimental Results

The 3D-ICs based on TSV technique have been proposed to overcome current limitations in manufacturing process of IC by stacking multiple dies via hundreds to thousands inter-die interconnection (TSVs). New proposed technique includes failure affect the system reliability and yield. To improve the repair process, a bundle of N TSVs is divided into set with spare ones. This leads to a much higher number of repairable faulty TSVs [11]. Furthermore, in the proposed approach, the spare TSVs are shared among all TSV clusters, the reparability rate R (the probability of successful repair) for data bundles in the multi defective TSVs that includes the uncorrelated TSV faults is:

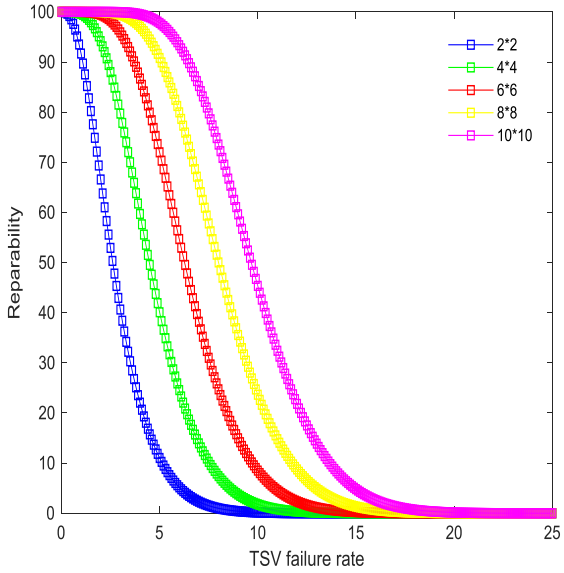


Fig. 8. Impact of spare TSV number on the reparability rate.

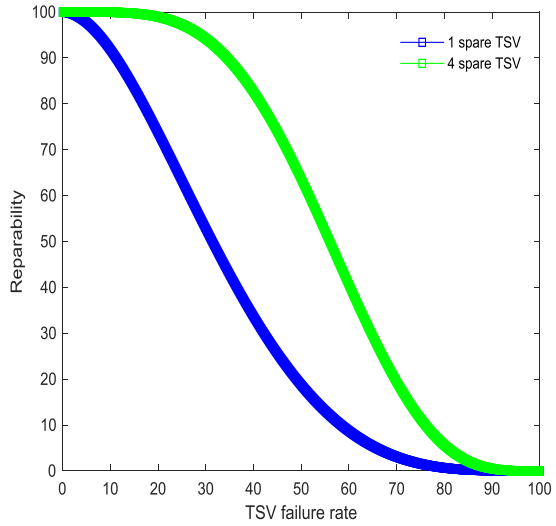
$$R=\sum_{k=N}^{N+r}\binom{N+r}{k}\left(1-D_{TSV}\right)^{k} D_{TSV}^{\,N+r-k} \quad (1)$$

Where D_{TSV} is the failure rate for single TSV.

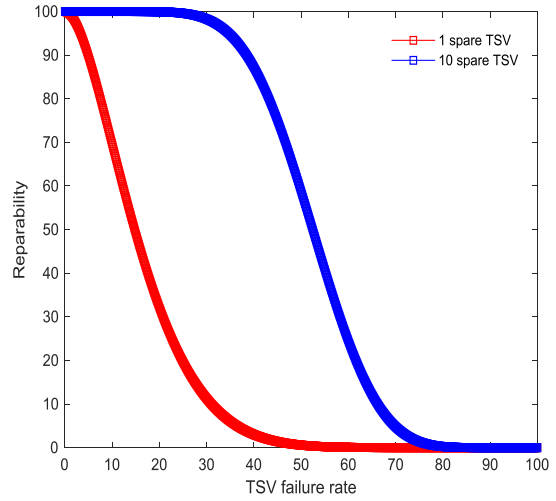
Fig. 8 presents the reparability and repair group for growing number of spares and rates of failure for N equal to 100 regular TSVs. For each repair group, there is one redundant TSV, while for two groups there are two spare TSVs and for ten groups there is ten spare. It can be concluded that the number of spare TSVs has a high impact to achieve higher reparability in- repair group.

In this repair architecture of multi defectives TSVs, data is transmitted in two-bundles whose can increase the reparability of circuit. For example, a group that consist of a set of four TSVs with one spare and in case of two defective TSVs, (Fig. 9(a)) two faulty free TSVs and one spare. With this solution, the total of spare TSVs is four. This is because partition of data in two- bundle give us in the first bundle one spare TSVs and in the second we can use all existing TSVs (two faulty free ones plus the redundant TSV) as spare then total of spare becomes four. In addition, the same for Fig. 9(b) in case of set of teen TSV.

The proposed test architecture was implemented in FPGA Virtex 5 ML 507 to extract the synthesis results. Tables I and II summarize the synthesis results of test UNIT architecture and the BISR, respectively. The tables show the number of slice registers, number of occupied Slice Lookup tables (LUTs), number of occupied slices and number of LUT Flip Flop pairs used in a various number of data bits of both proposed architecture.



(a)



(b)

Fig. 9. Reparability rate based on proposed repair methodology of group TSVs.

TABLE I. SYNTHESIS RESULTS OF TEST UNIT (IBIST)

Data Bits	Number of slices registers	Number of slices LUTs	Number of occupied slices	Number of LUT Flip Flop pairs used
4	46	23	17	54
8	82	39	29	96
16	154	64	50	176
32	298	115	100	339
64	586	177	204	680

TABLE II. SYNTHESIS RESULTS OF BISR

Data Bits	Number of slices registers	Number of slices LUTs	Number of occupied slices	Number of LUT Flip Flop pairs used
4	5	5	3	5
8	9	9	5	10
16	17	22	17	23
32	33	47	30	48
64	65	78	61	79

IV. CONCLUSION

In this paper, a novel repair process of a defective TSV in 3D-IC is presented. The proposed technique is based on two complimentary methods: IBIST for test, localization of faulty TSV and identify a kind the defects based on error signature, the second technique is BISR methodology for repair process. This last superpose to fault tolerance techniques, redundant TSV, and TDMA. In addition, the defective TSVs effectively isolated and repaired by a neighboring TSV of the proposed BISR structure. In case of multi defective TSVs, existing technique by dividing and transmitting data in two bundles to increase the reparability rate is improved based on TDMA technique. Experimental results and discussion show that the great yield improvement can be achieved (100% reparability for 30% of failure rate) with little area overhead penalty by using the proposed BISR structure.

REFERENCES

[1] L. W. Schaper, S. L. Burkett, S. Spiesshoefer, G. V. Vangara, Z. Rahman, and S. Polamreddy, “Architectural implications and process development of 3-D VLSI Z-axis interconnects using through-silicon vias,” IEEE Trans. Adv. Packag., vol. 28, no. 3, pp. 356–366, 2005.

[2] P. S. Andry et al., “Fabrication and characterization of robust through-silicon vias for silicon-carrier applications,” IBM J. Res. Dev., vol. 52, no. 6, pp. 571–581, 2008.

[3] R. S. Patti, “Three-dimensional integrated circuits and the future of system-on-chip designs,” Proc. IEEE, vol. 94, no. 6, pp. 1214–1224, 2006.

[4] J.-Q. Lu, “3-D hyperintegration and packaging technologies for micro-nano systems,” Proc. IEEE, vol. 97, no. 1, pp. 18–30, 2009.

[5] D. H. Jung et al., “Through silicon via (TSV) defect modeling, measurement, and analysis,” IEEE Trans. Compon. Packag. Manuf. Technol., vol. 7, no. 1, pp. 138–152, 2017.

[6] J. Li, X. Zhang, C. Zhou, J. Zheng, D. Ge, and W. Zhu, “New applications of an automated system for high-power LEDs,” IEEEASME Trans. Mechatron., vol. 21, no. 2, pp. 1035–1042, 2016.

[7] J. Li, L. Liu, L. Deng, B. Ma, F. Wang, and L. Han, “Interfacial microstructures and thermodynamics of thermosonic Cu-wire bonding,” IEEE Electron Device Lett., vol. 32, no. 10, pp. 1433–1435, 2011.

[8] C. Wang et al., “BIST methodology, architecture and circuits for pre-bond TSV testing in 3D stacking IC systems,” IEEE Trans. Circuits Syst. Regul. Pap., vol. 62, no. 1, pp. 139–148, 2015.

[9] Q. Xu, S. Chen, X. Xu, and B. Yu, “Clustered Fault Tolerance TSV Planning for 3-D Integrated Circuits,” IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 36, no. 8, pp. 1287–1300, Aug. 2017.

[10] A.-C. Hsieh and T. Hwang, "TSV redundancy: Architecture and design issues in 3-D IC," IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 20, no. 4, pp. 711–722, 2012.

[11] M. Nicolaidis, V. Pasca, and L. Anghel, "Through-silicon-via built-in self-repair for aggressive 3D integration," in On-Line Testing Symposium (IOLTS), 2012 IEEE 18th International, 2012, pp. 91–96.

[12] L. Jiang, Q. Xu, and B. Eklow, "On effective through-silicon via repair for 3-D-stacked ICs," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 32, no. 4, pp. 559–571, 2013.

[13] Y. Zhao, S. Khursheed, and B. M. Al-Hashimi, "Online fault tolerance technique for TSV-based 3-D-IC," IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 23, no. 8, pp. 1567–1571, 2015.

[14] Y.-G. Chen, W.-Y. Wen, Y. Shi, W.-K. Hon, and S.-C. Chang, "Novel spare TSV deployment for 3-D ICs considering yield and timing constraints," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 34, no. 4, pp. 577–588, 2015.

[15] C.-W. Chou, J.-F. Li, Y.-C. Yu, C.-Y. Lo, D.-M. Kwai, and Y.-F. Chou, "Hierarchical test integration methodology for 3-D ICs," IEEE Des. Test, vol. 32, no. 4, pp. 59–70, 2015.

[16] D. Arumí, R. Rodríguez-Montañés, and J. Figueras, "Prebond testing of weak defects in TSVs," IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 24, no. 4, pp. 1503–1514, 2016.

[17] J. Park, M. Cheong, and S. Kang, "R 2-TSV: A Repairable and Reliable TSV Set Structure Reutilizing Redundancies," IEEE Trans. Reliab., vol. 66, no. 2, pp. 458–466, 2017.

[18] W.-H. Hsu, M. A. Kochte, and K.-J. Lee, "Built-In Test and Diagnosis for TSVs With Different Placement Topologies and Crosstalk Impact Ranges," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., 2017.

[19] J. Park, H. Lim, and S. Kang, "FRESH: A New Test Result Extraction Scheme for Fast TSV Tests," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 36, no. 2, pp. 336–345, 2017.

[20] R. P. Reddy, A. Acharyya, and S. Khursheed, "A Cost-Effective Fault Tolerance Technique for Functional TSV in 3-D ICs," IEEE Trans. Very Large Scale Integr. VLSI Syst., 2017.

[21] S. Mondal, S.-B. Cho, and B. C. Kim, "Modeling and Crosstalk Evaluation of 3-D TSV-Based Inductor With Ground TSV Shielding," IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 25, no. 1, pp. 308–318, 2017.

[22] SNUG Silicon Valley. (2015). High Speed TDMA. [Online].Available: https://www.synopsys.com/news/pubs/snug/2015/siliconvalley/ta07_maheshwari_pres_snps.pdf

[23] I. Ndip et al., "High-frequency modeling of TSVs for 3-D chip integration and silicon interposers considering skin-effect, dielectric quasi-TEM and slow-wave modes," IEEE Trans. Compon. Packag. Manuf. Technol., vol. 1, no. 10, pp. 1627–1641, 2011.

[24] A. Sheibanyrad and F. Pétrot, "Asynchronous 3D-NoCs Making Use of Serialized Vertical Links," in 3D Integration for NoC-based SoC Architectures, Springer, 2011, pp. 149–165.

[25] F. Sun, A. Cevrero, P. Athanasopoulos, and Y. Leblebici, "Design and feasibility of multi-Gb/s quasi-serial vertical interconnects based on TSVs for 3D ICs," in VLSI System on Chip Conference (VLSI-SoC), 2010 18th IEEE/IFIP, 2010, pp. 149–154.University Science, 1989.